SERVICE MANUAL

C-128/C128D COMPUTER

NOVEMBER 1987 **PN-314001-08**

Commodore Business Machines, Inc.
1200 Wilson Drive, West Chester, Pennsylvania 19380 U.S.A.

CONTENTS

COMMODORE 128 | PERSONAL COMPUTER

GENERAL FEATURES	• Advanced Styling • 100% Compatible with Commodore 64 • Built-in, Easy to Use DOS support • RAM Expandable up to 512K RAM Using RAM Disk Option • Upper and Lower Case Character Set • Built-in BASIC • 3 Separate Modes of Operation
64 MODE	• 8502 Microprocessor (6502/6510 Compatible) • 6581 Sound Interface Chip • 64K RAM • 16K ROM • BASIC 2.0 • 40 x 25 Lines (320 x 200 resolution) • 16 Colors + 8 Sprites
128 MODE	• 8502 Microprocessor (6502/6510 Compatible) • 6581 Sound Interface Chip • 128K RAM (Expandable to 512K Using RAM Disk Option) • 48K ROM + 16K ROM for DOS Support • BASIC 7.0 • Machine Language Monitor • 40 x 25 Lines (320 x 200 resolution) • 80 x 25 Lines (640 x 200 resolution) • 16 Colors + 8 Sprites (40 Column Only)
CP/M MODE	• Z80 Microprocessor • CP/M™ Plus Version 3.0 • 128K RAM (Expandable to 512K Using RAM Disk Option) • 40 x 25 Lines (320 x 200 resolution) • 80 x 25 Lines (640 x 200 resolution) • 16 Colors
KEYBOARD	• Full Size Typewriter Style • 92 Keys • 14 Key Numeric Keypad • 8 Programmable Function Keys • 6 Cursor Keys • Help Key • 40/80 Column Key • No Scroll • Line Feed • Escape • Tab • Cap Lock • Alt (Not all accessible in 64 Mode)
INPUTS/OUTPUTS	• User Port • Cassette Port • RF/TV Port • Audio Input • Composite Video • Serial Port • 2 Game Ports • Cartridge Port • Audio Output • Digital RGBI Video
RECOMMENDED PERIPHERALS	• MPS 802, MPS 803, MPS 1000 Printers • 1541, 1571 Single Disk Drive • 1901 Monochrome Monitor • 1902 Digital RGBI Color Monitor • 1660 and 1670 Modems • Fully Compatible with Commodore 64 Software and Accessories in 64 Mode
POWER REQUIREMENTS	• 117 Volts AC, 60 Hz, 15 Watts

†Specifications subject to change without notice
*CP/M is a registered trademark of Digital Research, Inc.

PARTS LIST
C-128

PLEASE NOTE: Commodore part numbers are provided for reference only and do not indicate the availability of parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Approved cross-references for TTL chips, Transistors, etc. are available in manual form through the Service Department. Unique or non-standard parts will be stocked by Commodore and are indicated on the parts list by a "C".

TOP CASE ASSY

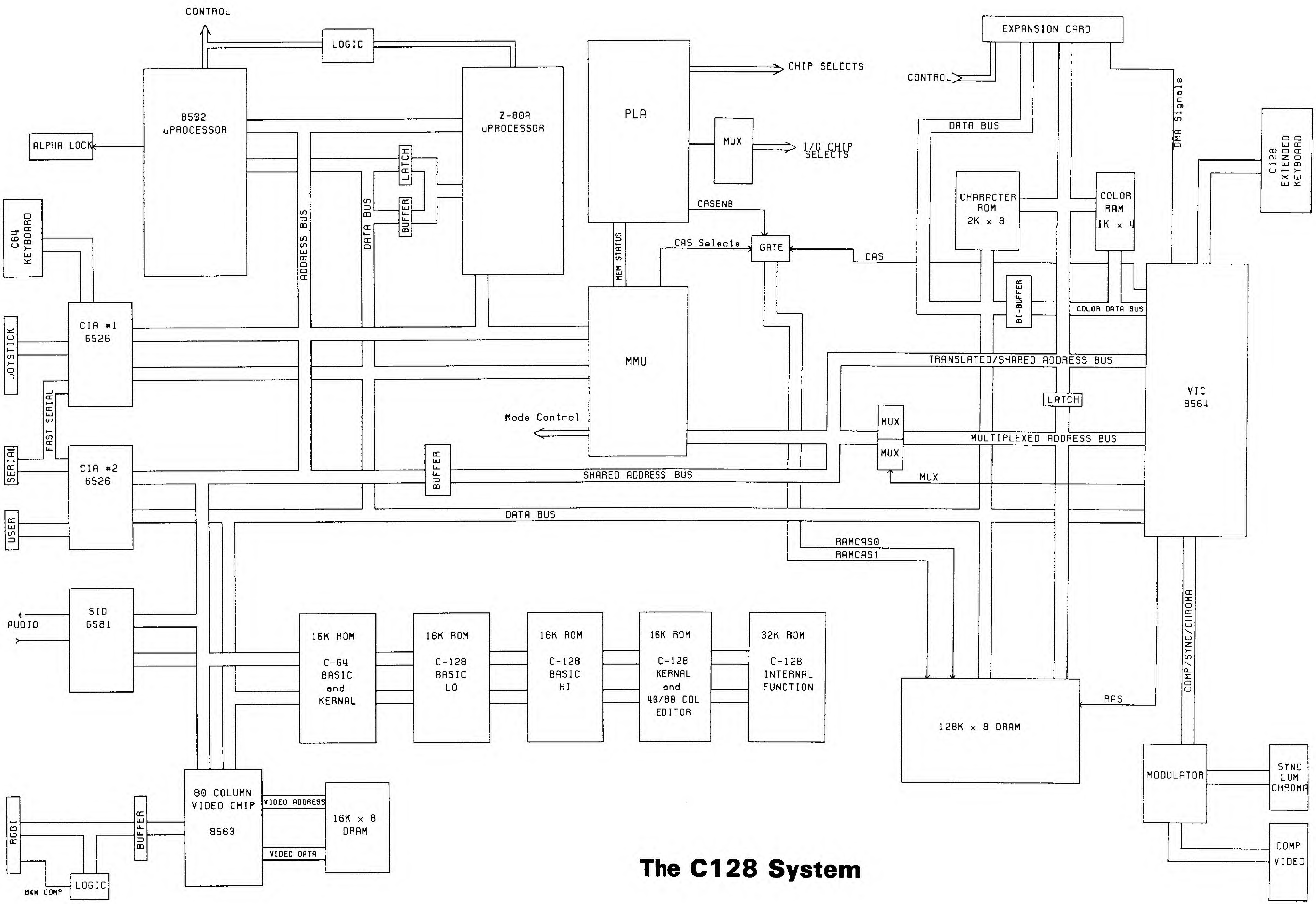
Top Case	C 251987-01
Keyboard	C 310401-01
Nameplate	C 310400-01
Lamp Holder Set	C 252013-01
LED Assembly	C 250754-01

BOTTOM CASE ASSY

Bottom Case	C 251988-01
Foot, Self-Adhesive	C 251993-01
PCB Top Shield	C 252015-01
PCB Bottom Shield	C 252016-01
PCB Insulation Sheet	C 252017-01

ACCESSORIES

Users Manuals	
Introductory Guide	C 319773-01
System Guide	C 310638-01
Power Supply	C 310416-01
RF Cable	C 326189-01
Switch Box	C 904778-01
Tutorial Diskette	C 317667-01
CP/M Diskette #1	C 317430-01
CP/M Diskette #2	C 317431-01



The C128 System

BUS ARCHITECTURE

FOLD OUT SCHEMATIC PAGES 73-76 FOR EASY REFERENCE.

The Processor Bus

The **Processor Bus** is the data and address buses that are directly connected to the 8502 processor. These buses are designated D_0 - D_7 for the eight bit data bus and A_0 -A_{15} for the sixteen bit address bus. These buses tie the processor to most of the system ROM and I/O devices, including at least part of all System ROM, all built-in Function ROM, the MMU, the PLA, the 8563 Video Processor, the SID, and both CIA chips.

The Processor Bus is in direct communication with the Z-80 co-processor as well. All address lines are shared directly by both processors. In order to allow the Z-80 to operate on a 6502 family bus, it is necessary to latch data going into the Z-80 and gate the data leaving the Z-80. Thus, the Z-80 has a small local data bus, designated ZD_0 -ZD_7. During a write cycle, when AEC is high, Z-80 data is gated to the Processor Bus. During a read cycle, Processor Bus data is gated to the Z-80 data bus. This read data is transparently latched by the 1 MHz system clock.

The read and write cycles referred to are, unless otherwise specified, 8502 type bus cycles. The Z-80 Read Enable and Write Enable outputs are conditioned using logic to interface with an 8502 bus cycle, so no distinction is made as to the differences between cycles of the different processors.

As mentioned above, the Z-80 is not in direct communication with the Processor Data Bus, due to the necessity of adapting the Z-80 to 8502 bus protocol. Note, however, that every other device and the translated bus (except two that will be explained later) shares the Processor Data Bus as a common data bus.

The Translated Address Bus

Another C128 system bus is the **Translated Address Bus**, which is produced by the MMU during AEC high. This bus consists of only high order addressing lines, designated TA_8 - TA_{15}. These lines reflect the action of the MMU on the normal high order address lines, which may or may not include some sort of translation. The MMU can translate the address of page zero or page one in normal operation, and it translates the Z-80 address from $0000 thru $0FFF in order to direct it to read the Z-80 BIOS. A more complete description of MMU translations can be found in the MMU section. Normally the Translated Address Bus indirectly drives the DRAMs and the VIC chip by driving the Multiplexed Address Buses. It directly drives System ROM 4 address line 12 to allow the Z-80 ROM relocation. Finally, this bus becomes address lines 8 thru 15 of the C64 compatible expansion port.

During a VIC cycle or a DMA, the MMU pulls TA_{12} - TA_{15} high, while TA_8 - TA_{11} are tri-stated. This allows the VIC chip to drive TA_8 - TA_{11} as VIC addresses VA_8 - VA_{11}.

The Multiplexed Address Bus

This section actually describes two related address buses, the **Multiplexed Address Bus** and the **VIC Multiplexed Address Bus**, known respectively as MA_0 - MA_7 and VMA_0 - VMA_7. The VIC Multiplexed Address Bus is created during AEC high by multiplexing the high order Translated Address Bus (TA_8 - TA_{15}) with the low order Processor Address Bus (A_0 - A_7), controlled via the MUX signal. This bus, driven though series resistors, is called the Multiplexed Address bus. The VIC Multiplexed Address Bus is used in addressing the VIC chip registers while the Multiplexed Address Bus is the processor's DRAM address for both 64K banks of DRAM.

During a VIC cycle, AEC low, the VIC chip address lines must be asserted. There is no completely separate address bus for the VIC addresses, so it shares the VMA_0 - VMA_7 and TA_8 - TA_{11} address lines that are otherwise tri-stated during AEC low. Most of the VIC addresses come out of the VIC chip already multiplexed, but two of them, VA_6 and VA_7. They do not supply column information, as the VIC chip supplies only fourteen bits of addressing. The higher order address bits VA_{14} and VA_{15} come from CIA 2, as in the C64. Thus, the VIC supplies complete VMA_0 - VMA_7 for a VIC DRAM access or DRAM refresh. The TA_8 - TA_{11} supplied by VIC are used in conjunction with another addressing bus for non-multiplexed VIC cycle addresses, such as Character ROM and Color RAM accesses.

The Shared Address Bus

The **Shared Address Bus** is a non-multiplexed address bus used by both the processor and the VIC chip. This is necessary to communicate with common resources, namely the Character ROM and Color RAM. During AEC high, the Shared Address Bus, designated SA_0 - SA_7, is driven by A_0 - A_7, the lower order Processor Address bits. The higher order bits needed are supplied by the Translated Address Bus, which is also a shared address bus. Thus, the processor is able to access both shared items.

During AEC low, the VIC addresses VA_0 - VA_7 (VMA_0 - VMA_7) must come onto the Shared Address Bus. Since VA_0 - VA_6 are actually multiplexed, the row address only must be sent to the Shared Address Bus. Thus, the Multiplexed VIC addresses are transparently gated when either $\overline{RAS}$ or MUX are low, but latched when both are high, which would indicate that a column address is about to be presented. The high order address bits, as well, are supplied by the shared Translated Address Bus. Note that the Shared Address Bus provides the lower eight bits of the expansion port address, allowing VIC access to cartridges and some additional drive capability by way of the TTL chips used to drive the Shared Address Bus.

The Color Data Bus

The Color RAM is written to or read from by a nybble data bus called the **Color Data Bus.** During AEC high, the Color Data Bus is connected to the lower half of the Processor Data Bus via an analog switch, allowing the Processor full access to the Color RAM. During AEC low, that switch is opened, effectively isolating the Color Data Bus from the Processor Data Bus. In this state, it is driven by the VIC extended data bus D_8 - D_{11}.

The Display Bus

The Display Bus is a bus local to the 8563 Video Controller VIC chip, consisting of the **Display Address**, DA_0 - DA_7, and the **Bus Display Data Bus**, DD_0 - DD_7. This local bus supports the 8563 display RAM, which is completely isolated from the rest of the C128 system. The Display Address Bus is a multiplexed address bus providing addressing to the display DRAM. The Display Data Bus provides communication between this DRAM and the 8563. The 8563 also provides row and column strobes and dynamic refresh to this DRAM.

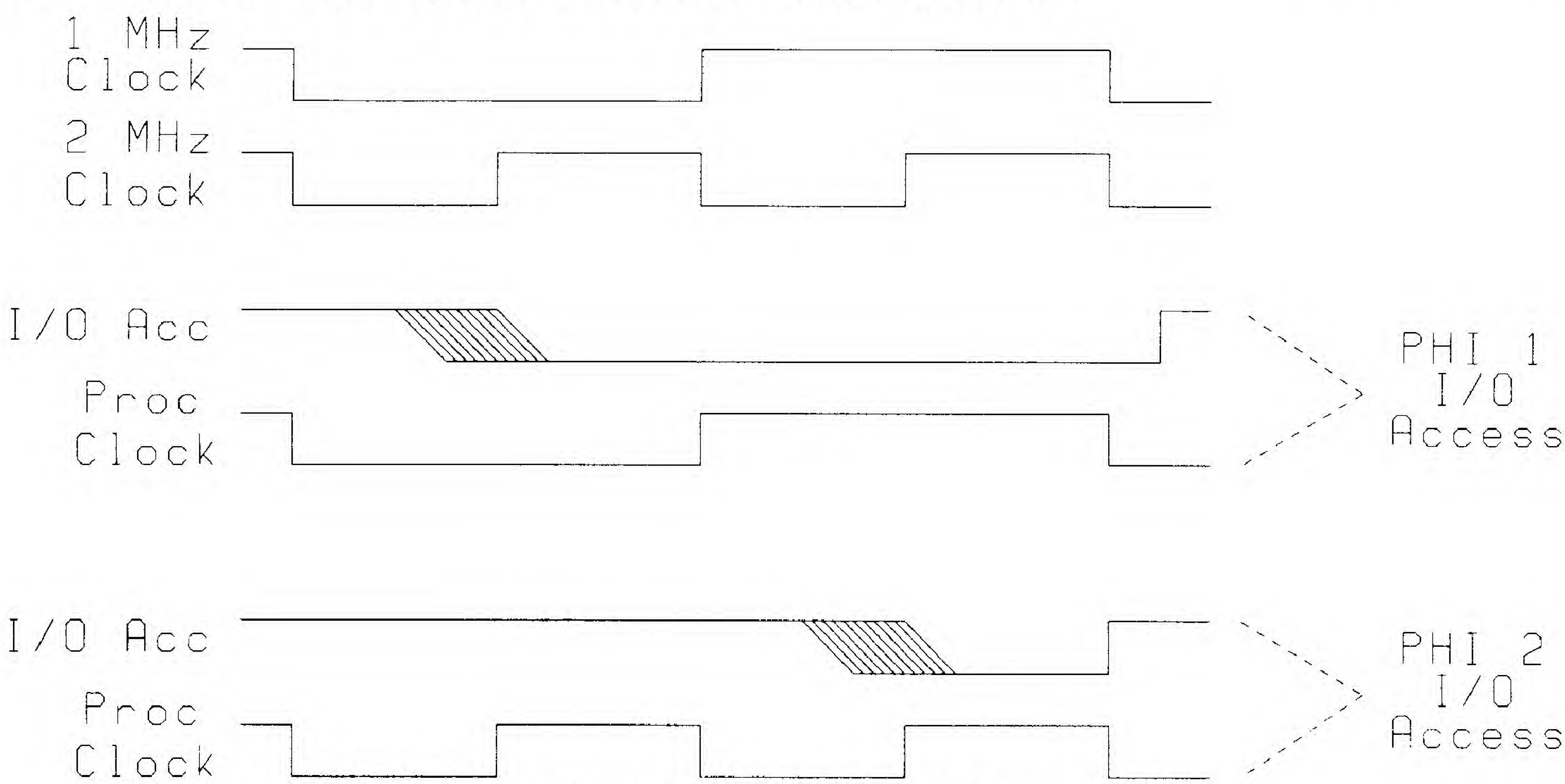
THE 8502 MICROPROCESSOR

FOLD OUT SCHEMATIC SHEET 2, PAGE 74, FOR EASY REFERENCE.

The 8502 is an HMOSII Technology microprocessor similar to the 6510/6502. It is the normal operating processor and is used in the C64 and the C128 modes. Fully software compatible with the 6510, hence the 6502, the 8502 also features a zero page port used in memory management and cassette implementations. The 8502 is also specified for operation at 2 MHz. The 2 MHz operation is made possible by removing the VIC from the system. The VIC chip is never completely removed from the C128 system, as it continues to function as clock generator and bus arbitrator. However, the VIC is removed as a display chip and co-processor, thus the full clock cycle can be devoted to processor functioning instead of sharing the cycle with the VIC. The task of video display processor is then taken over by the 8563, which can function without the need for bus sharing that the VIC required. Since the I/O devices, SID, etc., are rated at 1 MHz only, stretching of the 2 MHz clock is used to allow these parts to be directly accessed by the 2 MHz processor, and still keep throughput to a maximum. The I/O devices are not affected by the 2 MHz operation as they are still driven by a 1 MHz source (and as such, all timer operations remain unchanged), and clock stretching is only used to synchronize the 2 MHz machine cycle to the 1 MHz ϕ_0 high time. The clock sources and clock stretching capabilities are generated by the VIC chip.

CLOCK STRETCHING

When running in 2 MHz mode, the processor clock sometimes must be stretched. This is handled by the VIC chip, the processor, and the PLA working together. When an I/O operation is decoded during a 2 MHz cycle, the phase relationship between the 2 MHz and the 1 MHz clocks must be considered. If the 2 MHz access occurs during 1 MHz ϕ_1, the access to a clocked I/O chip would be out of synchronization with the 1 MHz clock that drives all I/O chips. Thus, during this phase relationship, $\overline{\text{IOACC}}$, from the PLA, signals the VIC chip to extend the 2 MHz clock. Should the 2 MHz cycles take place during the 1 MHz ϕ_2 cycle, no special attention is necessary.



Clock Stretching in 2 MHz Mode

Please take note to consider the speed implications of this. In 2 MHz mode, half of the I/O accesses given will occur at an effective speed of 1 MHz. For time critical operations, then, accesses to I/O chips are kept at a minimum.

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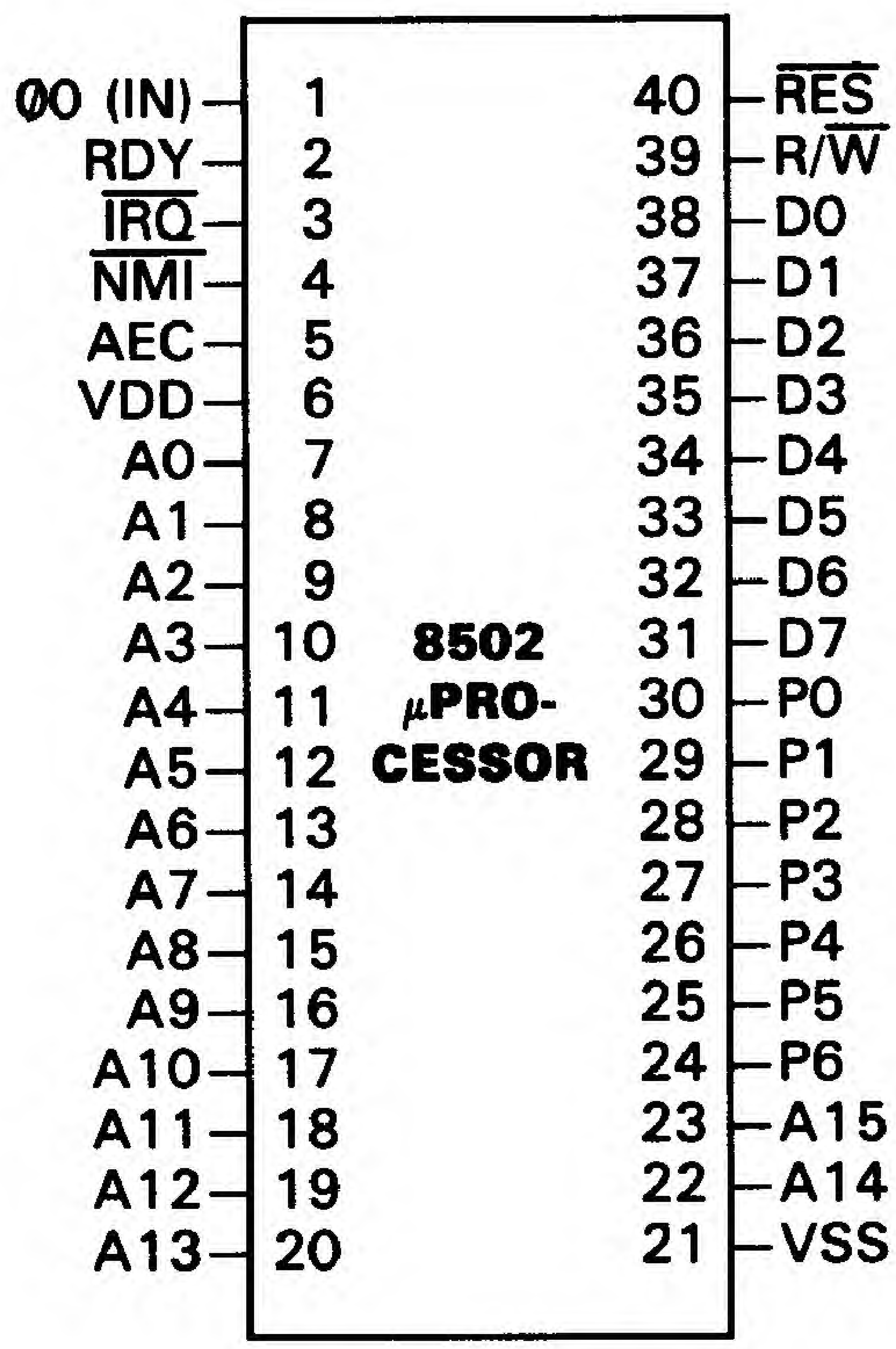
8502 MICROPROCESSOR



1	ØO	Phase 0 clock input. This is the dual speed system clock for the 128.
2	RDY	Ready. TTL level input, used to DMA the 8502. The processor operates normally while RDY is high. When RDY makes a transition to the low state, the processor will finish the operation it is on, and any subsequent operation if it is a write cycle. On the next occurrence of read cycle the processor will halt, making it possible to tri-state the processor to gain complete access to the system bus.
3	IRQ	The Interrupt Request input is a request that the processor initiate an interrupt sequence. The processor will complete execution of the current instruction before recognizing the request. At that time, the interrupt mask in the Status Code Register will be examined. If the interrupt mask is not set, the processor will begin an interrupt sequence. The Program Counter and the Processor status register will be stored on the stack and the interrupt disable flag is set so that no other interrupts can occur. The processor will then load the program counter from the memory location $FFFE and $FFFF.
4	NMI	The Non-Maskable Interrupt Request is a negative-edge sensitive request that the processor initiate an interrupt sequence. The processor will complete execution of the current instruction before recognizing the request. The Program Counter and the processor status register will be stored on the stack. The processor will then load the program counter from the memory locations $FFFA and $FFFB.
5	AEC	The Address Enable Control. The Address Bus is only valid when the AEC line is high. When low, the address bus is in a high impedance state. This allows DMA's for dual processor systems.
6	VDD	5VDC input.
7-20 22,23	A0-A15	Address bus outputs. Unidirectional bus used to address memory and I/O devices. The address bus can be disabled by controlling the AEC input.
21	VSS	DC ground.
24-30	P0-P6	Bidirectional I/O port used for transferring data to and from the processor directly. The Data Register is located at location $0001 and the Data Direction Register is located at location $0000.
31-38	D0-D7	Bi-directional bus for transferring data to and from the device and the peripherals.
39	R/W	The read/write line is a TTL level output from the processor to control the direction of data transfer between the processor and memory, peripherals, etc. This line is high for reading memory and low for writing.
40	RES	The Reset input is used to reset or start the µprocessor from a power down condition. During the time that this line is held low, writing to or from the µprocessor is inhibited. When a positive edge is detected on the input, the µprocessor will immediately begin the reset sequence. After a system initialization time of 6 cycles, the mask interrupt flag will be set and the processor will load the program counter from the contents of the memory locations $FFFC and $FFFD. This is the start location for program control. After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least 2 cycles. At this time the R/W line will become valid.

THE Z-80 MICROPROCESSOR

FOLD OUT SCHEMATIC SHEET 2, PAGE 74, FOR EASY REFERENCE.

The Z-80 microprocessor is used as a secondary processor in the C128 to run CP/M based programs. The Z-80 is interfaced to the 8502 bus and can access all of the devices that the 8502 can access.

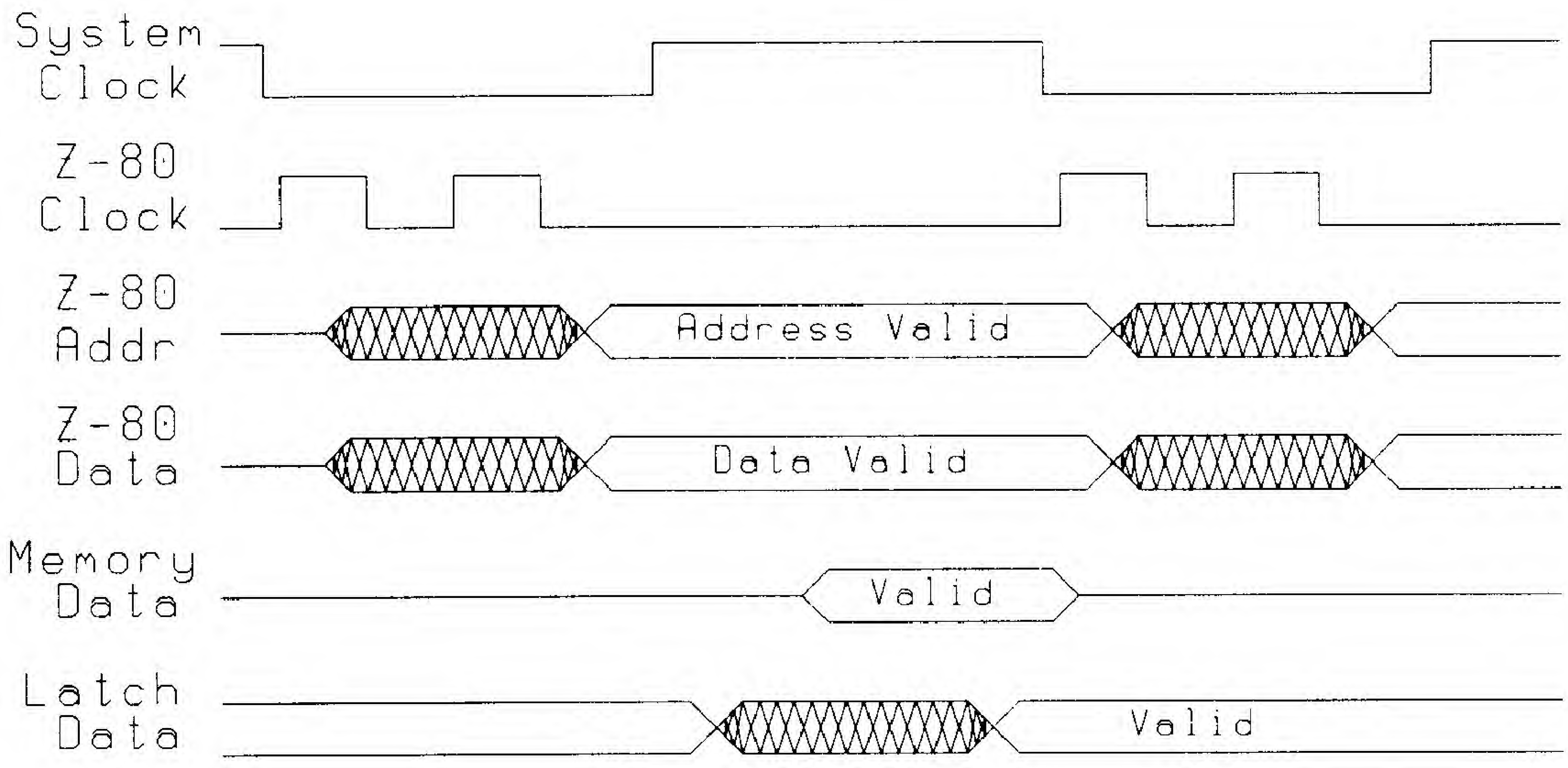
Bus Interface

Since a Z-80 bus cycle is much different than a 65xx family bus cycle, a certain amount of interfacing is required for a Z-80 to control a 65xx type bus. Since the Z-80 has built-in bus arbitration control lines, it is possible to isolate the Z-80 by tri-stating its address line. Thus, the Z-80 and 8502 both share common address lines.

The data lines do not interface quite as easily. Due to the shared nature of the bus during Z-80 mode, it is necessary to isolate the Z-80 from the bus during AEC low. Thus, a tri-stable buffer must drive the Processor bus during Z-80 data writes. The reverse problem occurs during a Z-80 read — the Z-80 must not read things that are going on during AEC low. It must latch the data that was present during AEC high. Thus, a transparent latch drives the data input to the Z-80. It is gated by the Z-80 Read Enable output, and latched when the 1 MHz clock is low. It will be seen that the Z-80 actually runs during AEC low, but that the data bus interfaces with it only during AEC high.

Control Interface

The Z-80 control interfacing must provide useful clock pulses to the Z-80 and must tailor the Z-80 Read and Write Enable signals for the 8502 type bus protocol. The Z-80 clock is provided by the VIC chip, and is basically a 4 MHz clock that only occurs during ϕ_0 low, as seen in the Z-80 bus timing diagram. This insures that the Z-80 is only clocked when it is actively on the bus. One additional problem that arises in clocking the Z-80 is that while all of the 8502 levels, and most of the Z-80 levels, are TTL compatible, the Z-80 clock input expects levels very close to five volts. For that reason, the ouptut from the VIC chip is processed by a transistor switching circuit to give a full amplitude clock. This circuit uses the nine volt supply, thus, the nine volt circuit **must** be operational for the Z-80 to function.



Z-80 Bus Timing

The Z-80 is designed to have explicit Read, Write and I/O cycles, where an I/O cycle is distinct from a memory cycle. The 65xx family uses only memory mapped I/O and thus, for a 65xx bus, all I/O devices appear as memory locations, and all non-write cycles appear as read cycles. The Z-80 communicates cycle information via two control lines, the Read Enable and Write Enable lines. The C128 uses the Read Enable line of the Z-80 to gate the Processor Bus data to the Z-80 data bus. The Write Enable interfacing is somewhat more complicated.

The Write Enable Circuitry consists of a rising-edge triggered D-Type flip-flop and an SR flip-flop. The D-flop is triggered by the rising-edge of the 1 MHz clock. The positive output of the SR drives the D-input, and the Q output gated with AEC drives an open collector inverter, which in turn drives the R/W line of the 8502 bus. The $\overline{\text{S}}$ input is driven by the Z-80 $\overline{\text{WE}}$, and the $\overline{\text{R}}$ input is driven by the Q output of the D-flop. Normally the D-input is low, resulting in an 8502 read cycle. When the Z-80 $\overline{\text{WE}}$ signal falls, it sets the SR flop, causing the D-input to rise. This line remains high, even if the Z-80 $\overline{\text{WE}}$ should rise again. When the 1 MHz clock rises, this high level is clocked, causing an 8502 write cycle that will last one complete 1 MHz cycle. When the Write signal is passed by the D-flop, the $\overline{\text{Q}}$ output will reset the SR flop. If no more $\overline{\text{WE}}$ signals come, the D-flop will once again set 8502 Read mode.

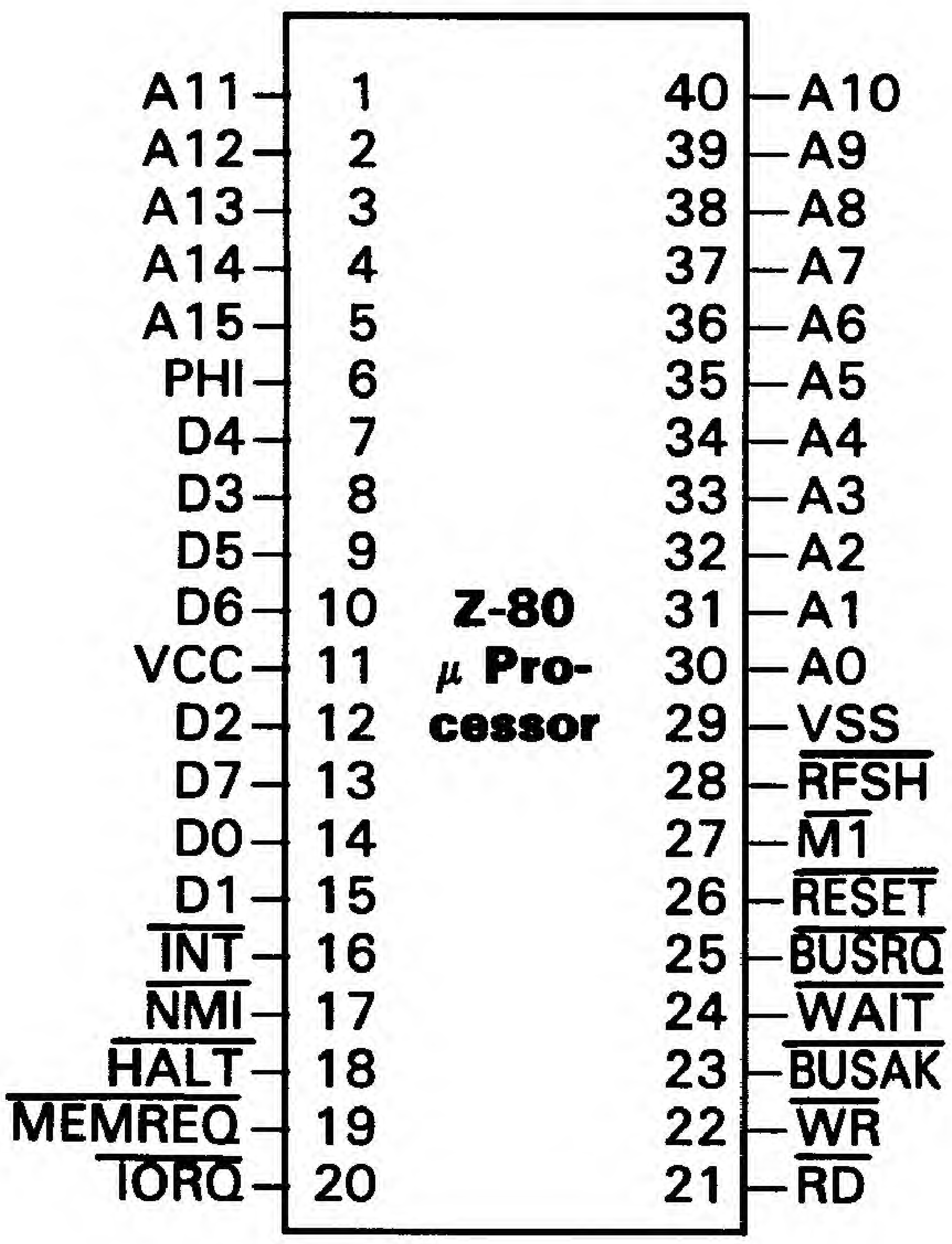
Processor Switching

It is important in normal operation for the Z-80 and 8502 to operate as co-processors, communicating between each other. This is, however, only serial co-processing, not to be considered parallel co-processing or multiprocessing. Only one processor may have the bus at any one time. This is important in several ways. First, the C128 system must power up with the Z-80 as the master processor. This is because the Z-80 will not power up cleanly, and may accidently access the bus when powering up. Thus, it is made master on powerup and can do anything it likes to the bus. Also, the Z-80 can start up certain C64 applications that would cause the 8502 to crash, thus again it is the logical choice for startup processor. After some initializations, the Z-80 will start up the 8502 in either C128 or C64 mode, depending upon if a cartridge is present.

The second reason for processor switching is to allow the Z-80 to access 8502 Kernal routines. For standardized programs, or for any I/O operation not supported in the Z-80 BIOS, the Z-80 can pass on the task of I/O to the 8502. Since the Z-80 sees BIOS ROM where the 8502 sees its pages 0 through F, the Z-80 can operate without fear of disrupting any 8502 pointers or the stack in RAM Bank 0.

The Z-80 can receive a bus grant request from the MMU, via $\overline{\text{Z80EN}}$, or from the VIC chip, via BA. Since the VIC control line is used for DMAs, that is not of immediate concern. The $\overline{\text{Z80EN}}$ action, however, is, since it is the mechanism by which processors swap control. When the $\overline{\text{Z80EN}}$ line goes high, it triggers a Z-80 $\overline{\text{BUSRQ}}$. The Z-80 will relinquish the bus by pulling $\overline{\text{BUSACK}}$ low. This action drives the 8502 AEC high and, providing VIC does not request a DMA, will also drive the 8502 RDY line high, enabling the 8502. To switch back, a low on the Z-80 $\overline{\text{BUSRQ}}$ will result in Z-80 $\overline{\text{BUSACK}}$ going high, tri-stating and halting the 8502.

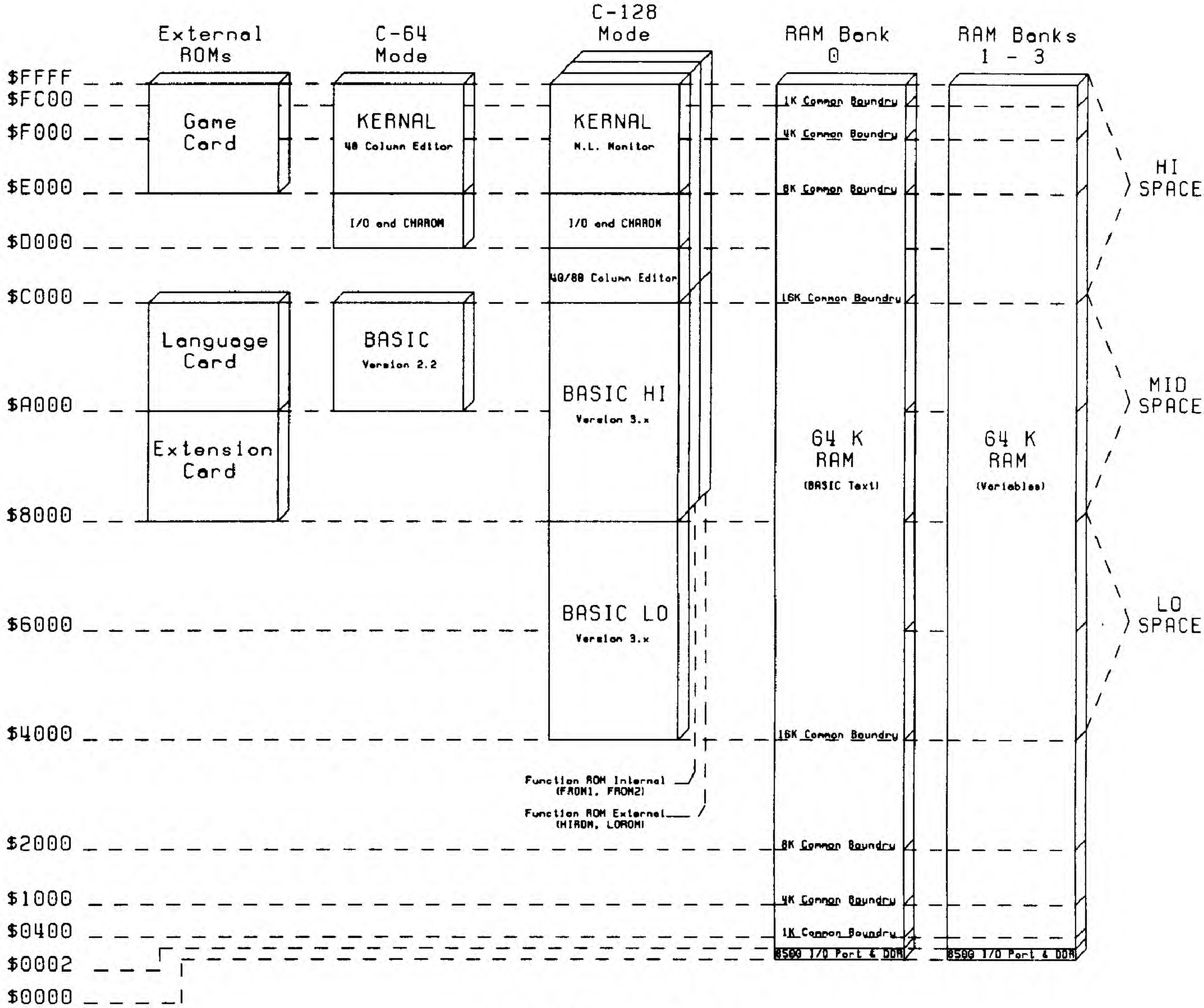
906150
Z-80 MICROPROCESSOR



1-5, 30-40	A0-A15	16 Bit tri-stating Address Bus. Used for 16 bit memory address during memory cycles, used for 8 bit I/O address during I/O cycles. This allows up to 256 input or 256 output ports. During refresh time, the lower 7 bits contain a valid refresh address.
6	PHI	Single phase system clock.
7-10, 12-15	D0-D7	Input/Output Data Bus, capable of tri-stating, used for 8-bit data exchanges with memory and I/O devices.
11	VCC	5VDC input.
16	INT	Interrupt Request. Active low input, driven by external devices. If the interrupt flag IFF is enabled, and the $\overline{BUSRQ}$ line is not active, the processor will honor the requested interrupt at the end of the current instruction. When the Z-80 acknowledges an interrupt, it generates an interrupt acknowledge signal ($\overline{IORQ}$ during M_1) at the beginning of the next instruction cycle. There are three different modes of response to a given interrupt.
17	NMI	Non-Maskable Interrupt. Active low input. This interrupt is edge triggered and cannot be masked against. It is always recognized at the end of the current instruction, forcing the Z-80 to take a restart at location $0066. The program counter is automatically saved in the stack to allow a return from the interrupted program. Note that continuous WAIT cycles can delay an $\overline{NMI}$ by preventing the end of the current cycle, and that $\overline{BUSRQ}$ will override $\overline{NMI}$.
18	HALT	Halt State. Active low output indicating that the Z-80 has executed a HALT instruction and is awaiting some kind of interrupt before execution can continue. While in the $\overline{HALT}$ state, the CPU continuously executes NOPs to continue refresh activity.
19	MEMREQ	Memory Request. Active low, tri-state output that indicates that the address bus holds a valid address for a memory read or write operation.
20	IORQ	Input/Output Request. Active low, tri-state output. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid address for an I/O read or write operation. An $\overline{IORQ}$ signal is also generated with an $\overline{M_1}$ signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. An interrupt can be acknowledged during $\overline{M_1}$; I/O operations never occur during $\overline{M_1}$.
21	RD	Memory Read. Active low, tri-state output. $\overline{RD}$ indicates that the CPU wants to read data from memory or from an I/O device. This signal is generally used to gate read data onto the data bus.
22	WR	Memory Write. Active low, tri-state output. $\overline{WR}$ indicates that the data bus holds valid data to be processed by memory or by an I/O device.
23	BUSAK	Bus Acknowledge. Active low output, used to indicate to any device taking over the bus that the Z-80 has gone into tri-state and the bus has been granted. While in this mode it cannot refresh dynamic memory.
24	WAIT	Wait. Active low input, used to drive the Z-80 into wait states. As long as this signal is low, the Z-80 will execute wait states, allowing this signal to be used to access slow memory and I/O devices. While the Z-80 is in a $\overline{WAIT}$ state, it cannot refresh dynamic memory.
25	BUSRQ	Bus Request. Active low input that is used to request the CPU address, data, tri-statable output control signals to all go tri-state for bus sharing and DMAs. The lines go tri-state upon termination of the current machine cycle.
26	RESET	Reset. Active low input which forces the program counter to zero and initializes the Z-80, which will set interrupt mode 0, disable interrupts, and set registers I and R to zero. During $\overline{RESET}$, address and data buses tri-state and all other signals go inactive.
27	M_1	Machine Cycle One. Output, active low. This signal indicates that the current machine cycle is the OP code fetch of an instruction execution. During execution of a two byte op-code, $\overline{M_1}$ is generated as each byte is fetched. $\overline{M_1}$ also occurs with $\overline{IORQ}$ to indicate an interrupt acknowledge cycle.
28	RFSH	Refresh. Active low output used to indicate that the address bus holds a refresh address in its lower seven bits. Thus, the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories not refreshed from an alternate source. A_7 is set to zero and the upper eight bits contain the I register at this time.
29	VSS	Ground.

MEMORY ARCHITECTURE

FOLD OUT SCHEMATIC PAGES 73-76 FOR EASY REFERENCE.



C128 Memory Map

C128 ROM Memory Organization

The memory map is an important consideration in maintaining C64 compatibility. The standard map is shown for the C64 mode. The C128 basically becomes a C64 when in C64 mode.

C128 mode is achieved at system reset, and is controlled by a bit in the MMU configuration register (See MMU Circuit Theory, page 20). In C128 mode, the MMU asserts itself in the C128 memory map at $FF00 and in the I/O space starting at $D500. Use of MMU registers, located at $FF00, allows memory management without actually having the I/O block banked in at the time and with a minimum loss of contiguous RAM. The MMU is removed from the memory map in C64 mode but is still used by hardware to manage memory.

The ROMs in C64 mode, both internally and externally, look just like C64 ROMs. The internal BASIC and KERNAL provide the C64 mode with the normal C64 operating system in ROM. This ROM actually duplicates some of the ROM used in C128 mode, but is necessary, as it is not accessible from C128 mode. In C128 mode, up to 48K of Operating System is present, with the exact amount being set by software control. This allows quicker access to underlying RAM by turning off unneeded sections of the Operating System.

The External ROMs represented on the memory map are those used in the C64 mode, and obey the C64 rules for mapping, i.e., cartridges assert themselves in hardware via the $\overline{\text{EXROM}}$ and $\overline{\text{GAME}}$ lines. External ROMs in C128 mode are mapped as banked ROMs, such that when the system is initialized, all ROM slots are polled for the existance of a ROM and the ROM's priority if one exists. This allows much more flexibility than the hardwire ROM substitution method, since the Kernal and Basic ROMs can be swapped out for an application program, swapped out for external program control, or turned off all together. This banking manipulation is accomplished by writing to the Configuration Register at location $D500 or $FF00, in the MMU.

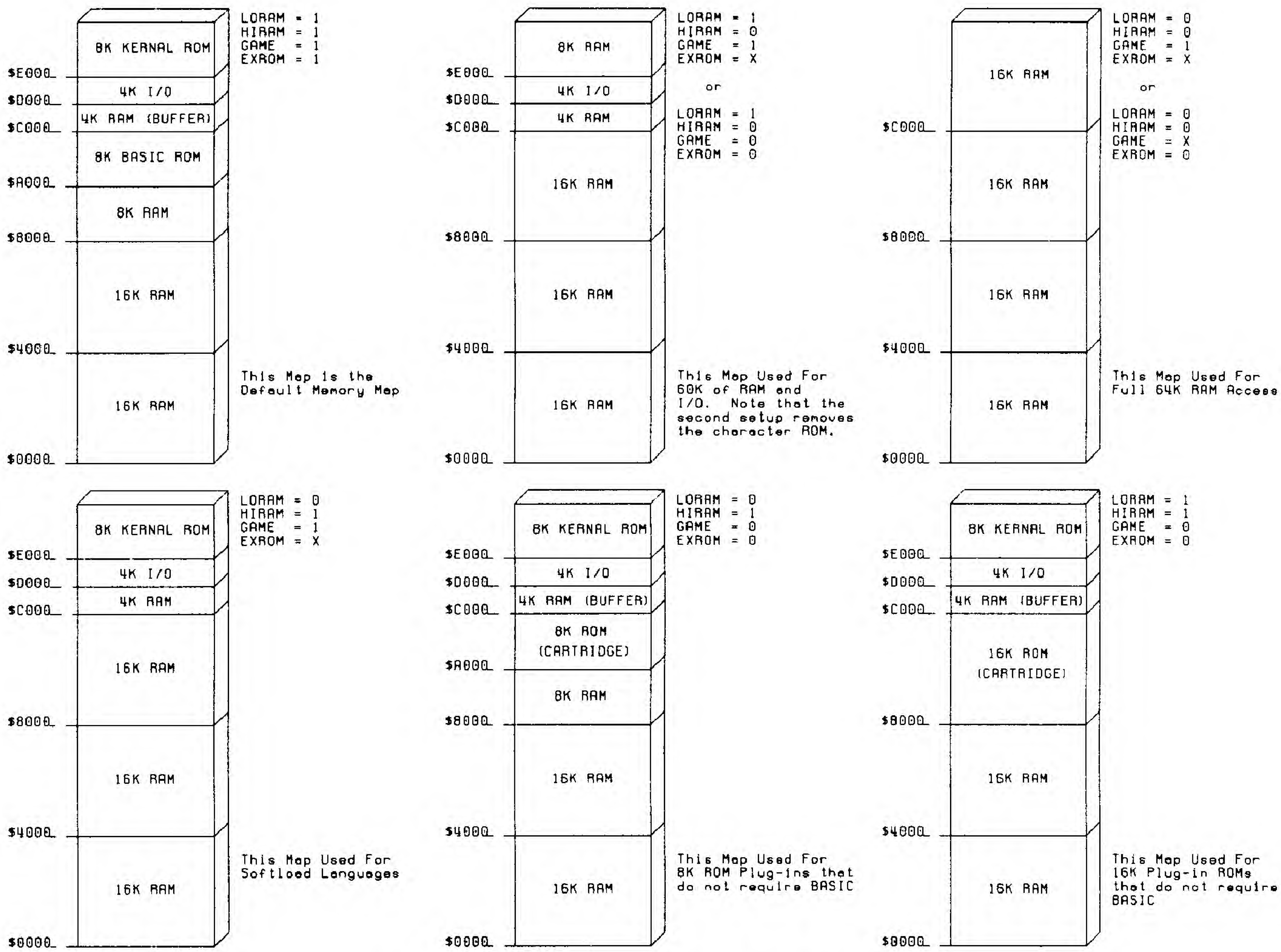
The hardware also features the ability to store preset values for the configuration and force a load of the Configuration Register by writing to one of the LCR (Load Configuration Register) registers.

C128 RAM Memory Organization

Refer again to the **C128 Memory Map.** The RAM present in the system is actually composed of two 64K by 8 bytes of contiguous DRAM. The RAM is accessed by selecting one of the two banks of 64K according to the RAM banking rules set in the RAM Configuration Register of the MMU. The area shown as RAM is representative of what the μProcessor would see if all ROM were disabled. Bank switching can be accomplished in one of two ways.

The bank in use is a function of the value stored in the Configuration Register. A store to this register will always take effect immediately. An indirect store to this register, using preprogrammed bank configuration values, can be accomplished by writing to one of the **indirect load** registers, known as **LCRs** (Load Configuration Register), located in the $FF00 region of memory. By writing to an LCR the contents of its corresponding PCR (PreConfiguration Register) will be latched into the configuration register. Refer to the MMU section on page 20 and the Alternate Memory Configurations on the following page.

When dealing with 64K banks of memory at once, it may be desirable to bank in bank 1 but still retain the system RAM (Stack, Zeropage, Screen, etc.). The MMU has provisions for what is referred to as **common RAM.** This is the RAM that does not bank, and is programmable in size and as to whether it appears at the top, bottom, or both in the memory map. The size is set by bits 0 and 1 in the **RAM Configuration Register (RCR).** If the value of the bits is zero, 1K will be common. Values of one, two, and three produce common areas of 4K, 8K, and 16K respectively. If bit 2 of the RCR is set, bottom memory is held common, if bit 3 is set, then top memory is common. In all cases, common RAM is physically located in bank 0.



C64 Alternate Memory Configurations

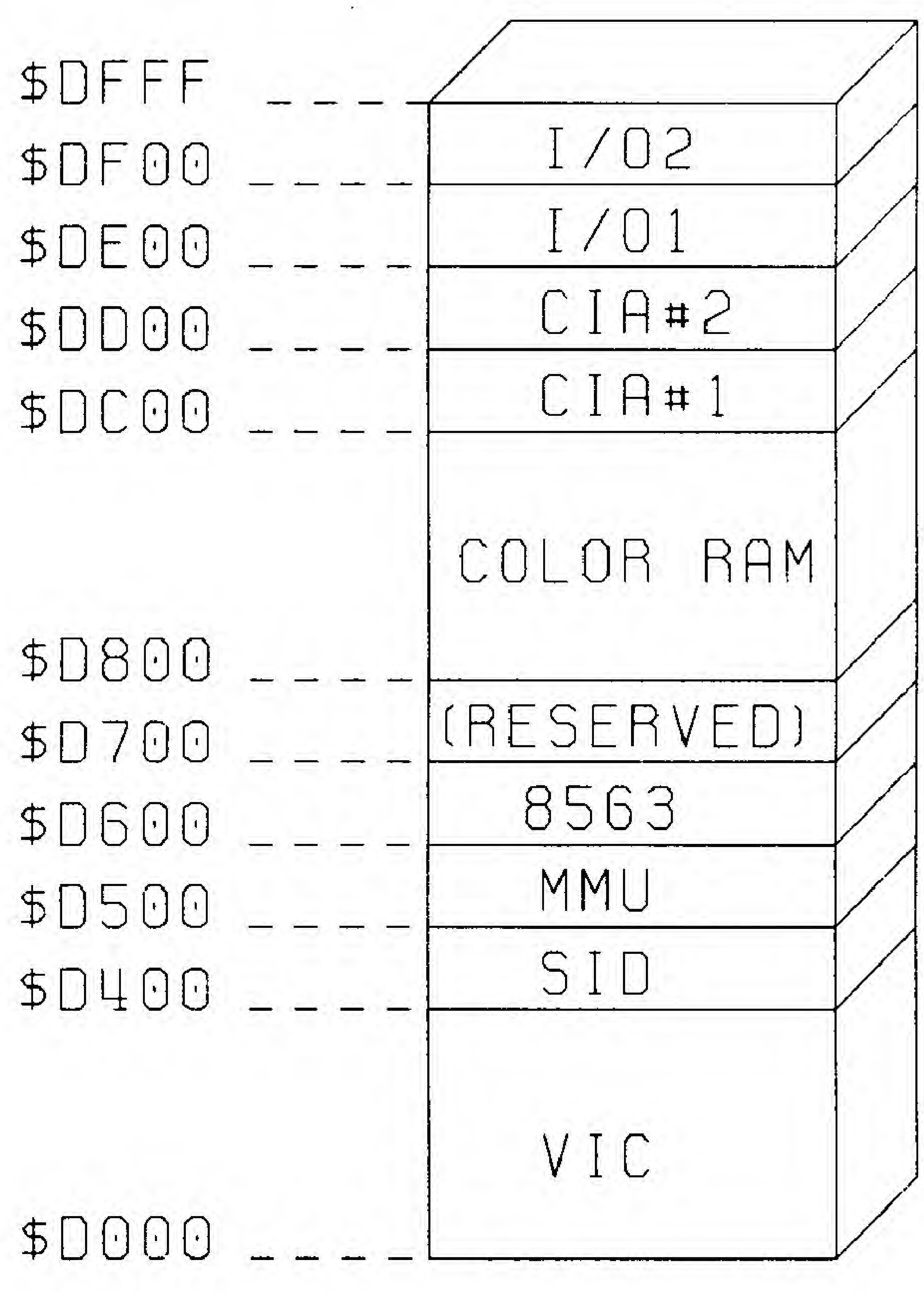
Zero page and page one can be located (or relocated) independently of the RCR. When the processor accesses an address that falls within zeropage or page one, the MMU adds to the high order μProcessor address, the contents of the P0 register pair or the P1 register pair, respectively, and puts this new address on the bus, including the extended addressing bit A_{16}. RAM banking will occur as appropriate to access the new address. Writes to the P0 and P1 registers will be stored in a prelatch, until a write to the respective P_{XL} register occurs. This prevents a P_{XH} register from affecting the translated address until both high and low bytes have been written.

At the same time, the contents of the P0 and P1 registers are applied to a digital comparator, and a reverse substitution occurs if the address from the 8502 falls within the page pointed to by the register. This results in not just relocating the zero or one page but swapping the zero or one page with the memory that it replaced. Swapping only occurs if the swapped area is defined as RAM, i.e., System or Function ROM must always be at their assigned addresses and thus should not be back-substituted. Note that upon system reset, the pointers are set to true zero and true one page.

For VIC chip access, one bit in the MMU status register is substituted for extended address line A16, selecting the proper CAS enable to make it possible to steer the VIC to anywhere in the 128K range. Note that AEC is the mechanism that the MMU uses to steer a VIC space address, i.e., when AEC is low a VIC access is assumed. This results in the VIC bank being selected as well for an outside DMA, since this too will pull the AEC line low.

MMU and I/O Memory Organization

The block of memory represented by the **I/O Block** is an expanded view of the memory block entitled **I/O + CHAROM**, as shown in the C128 memory map. When the I/O block exists, access to VIC, SID, and I/O, as well as the addition of the MMU can be accomplished. All I/O functions remain as they were previously on the C64 with the exception that the MMU and the 80 Column chip have been added. With the exception of four registers that are asserted in the zero page in C128 mode, all new MMU registers appear in an unused slot in the I/O Memory block, though they will only appear in C128 mode. Detailed descriptions of the MMU registers can be found in the MMU section on page 20.



I/O Block

READ ONLY MEMORY

FOLD OUT SCHEMATIC SHEETS 3 AND 4, PAGES 75 AND 76, FOR EASY REFERENCE.

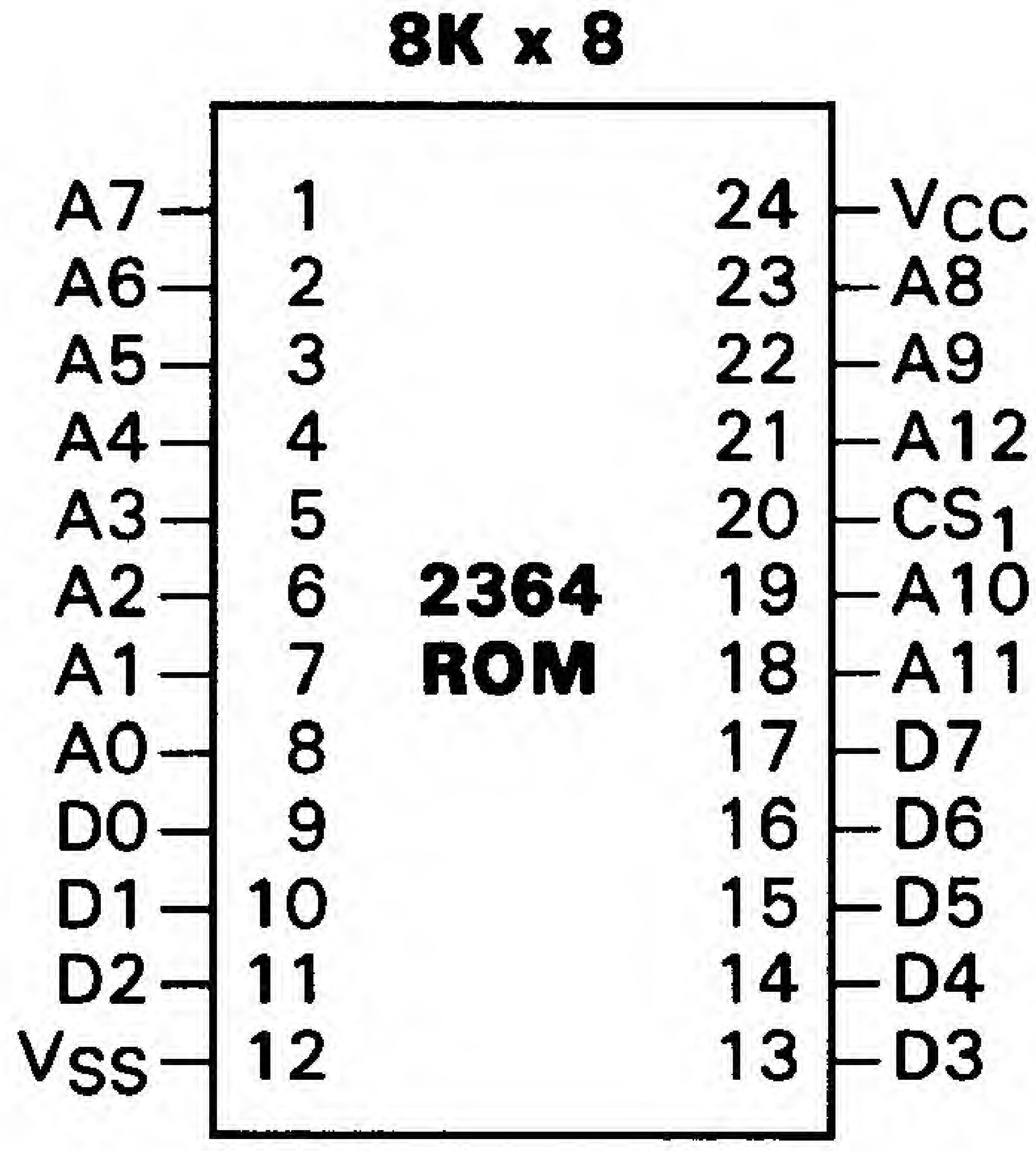
In C64 mode, the operating system resides in 16K of ROM, which includes approximately 8K for Kernal and 8K for Basic. In C128 mode, the operating system resides in 48K of ROM and includes advanced Kernal and Basic features. The Kernal, by definition, is the general operating system of the computer, with fixed entry points into usable subroutines. The entry table for the Kernal is located in memory at addresses $FF40 - $FFF9, exluding of course the MMU registers at $FF00 - $FF04. There is also a CHARACTER ROM, 8K x 8, which resides on the Shared Bus, shared by the VIC chip and the processor. The C64 OS ROM is wired so as to appear as two chunks of non-contiguous ROM, copying the actual C64 ROM memory map. Provision is included to handle system ROM as either four 16K x 8 ROMs or as two 32K x 8 ROMs. All internal C128 function ROMs will be the 32K x 8 variety.

Rom Banking

Refer to the **MMU Register Map** on page 20. Note that the Configuration Register (CR) controls the type of ROM or RAM seen in a given address location. Dependent on the contents of the CR, ROM may be enabled and disabled to attain the most useful configuration for the application at hand. ROM is enabled in three memory areas in C128 mode, each consisting of 16K of address space. The lower ROM may be defined as RAM or System ROM, the upper two ROMs may be System ROM, Function ROM, Cartridge ROM, or RAM. In C64 mode the C64 memory mapping rules apply, which are primitive compared to those used in C128 mode. C64 ROM is banked as two 8K sections, BASIC and KERNAL, according to the page zero port and the cartridge in place at the time. No free banking can take place when a cartridge is in place.

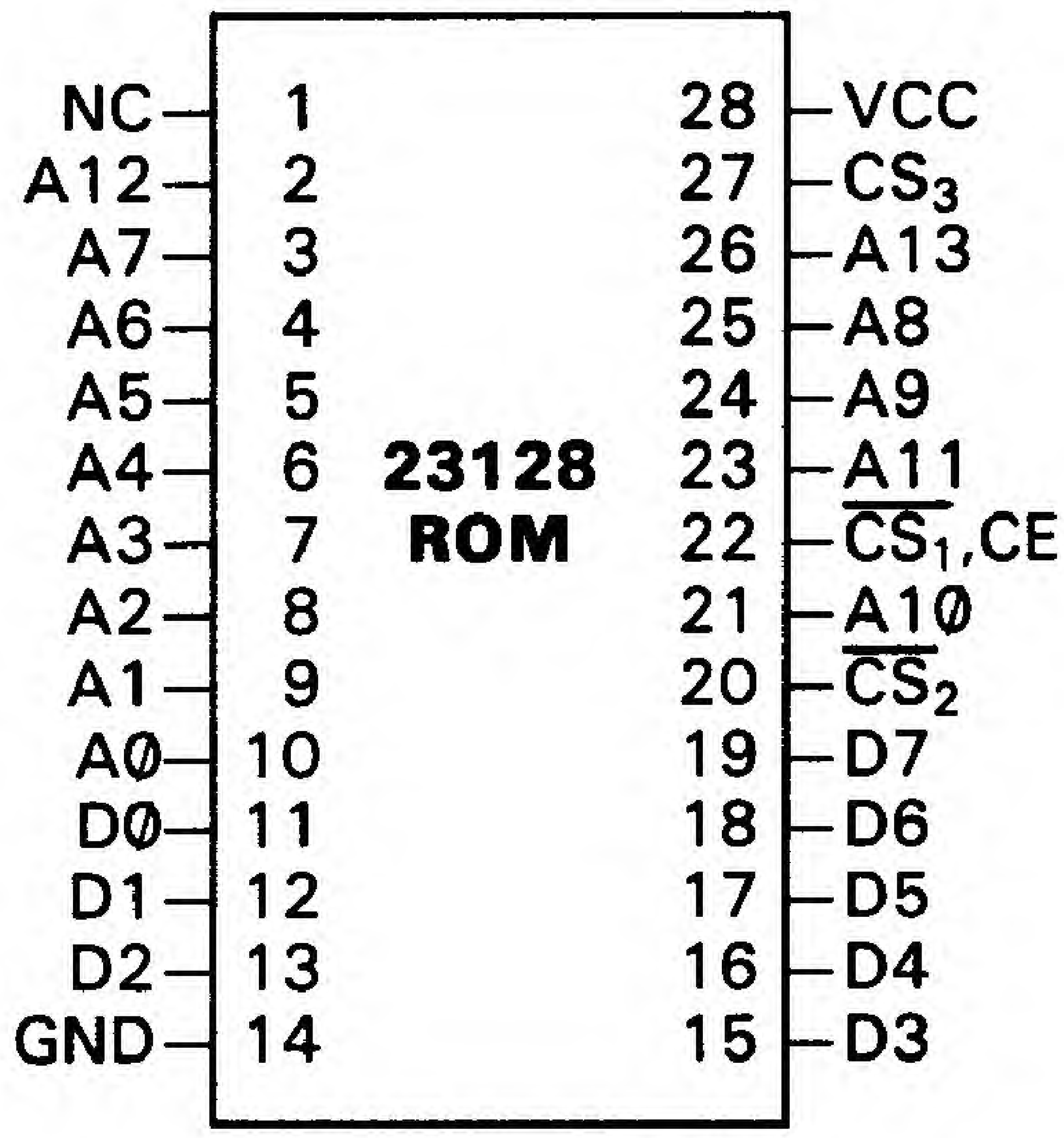
In the C128, if an address falls into the range of an enabled ROM, the MMU will communicate the status of ROM to the PLA decoder via the Memory Status lines. Essentially, the MMU looks up in the Configuration Register which ROM or RAM is set. The various combinations possible are shown on the **C128 Memory Map** found on page 11. The banking scheme, the way it is implemented, allows up to 32K of internal, bankable ROM for use such as Function Key Applications programs, and will support 32K of external bankable ROM. Various combinations of ROM are possible, and can be noted by studying the configurations for the Configuration Register.

8K x 8



1-8, 18,19, 21-23	A0-A12	Address Bus Inputs.
12	V_{SS}	Ground.
9-11, 13-17	D0-D7	Data Outputs.
20	CS_1	Chip Select.
24	V_{CC}	5VDC Input.

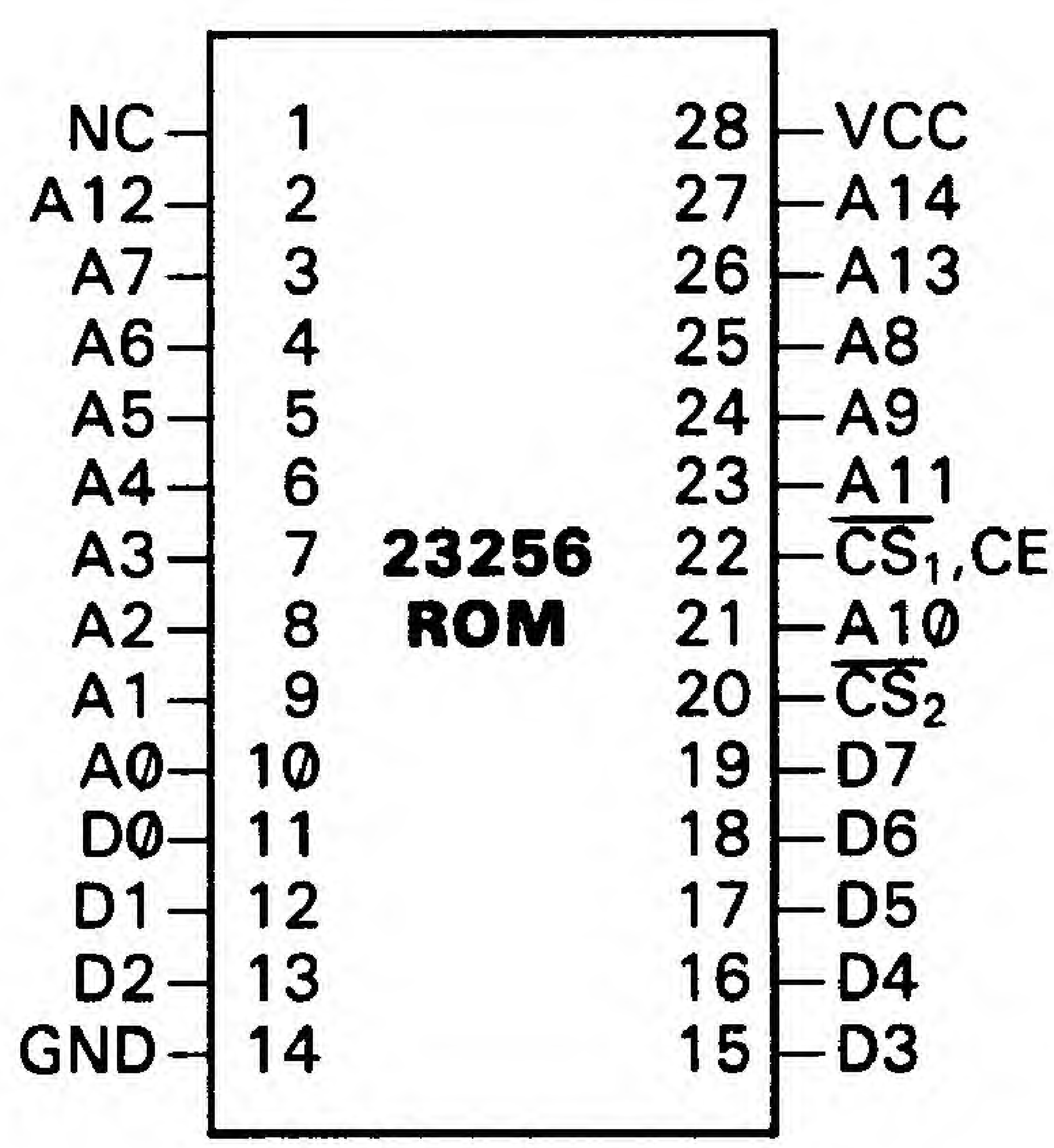
PIN CONFIGURATION



16K x 8 ROM

1	NC	Not Connected.
2-10, 21, 23-26	A0-A13	Address Bus Inputs.
11-13, 15-19	D0-D7	Data Outputs.
14	GND	Ground.
20	CS_2	Chip Select.
22	CS_1, CE	Output Enable.
27	CS_3	Program Enable.
28	VCC	5VDC Input.

PIN CONFIGURATION



32K x 8 ROM

1	NC	Not Connected.
2-10, 21, 23-27	A0-A14	Address Bus Inputs.
11-13, 15-19	D0-D7	Data Outputs.
14	GND	Ground.
20	CS_2	Chip Select.
22	CS_1, CE	Output Enable.
28	VCC	5VDC Input.

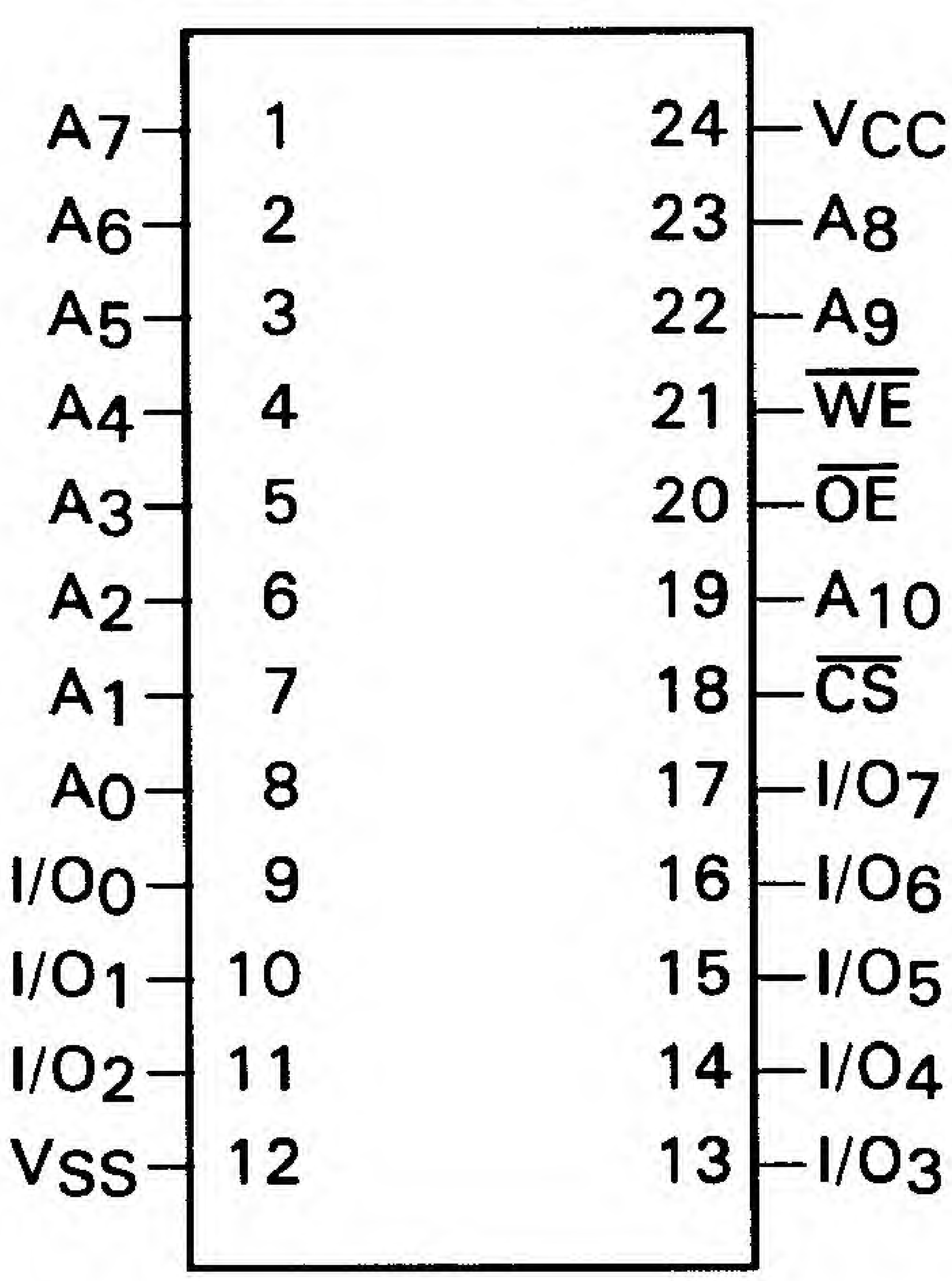
RANDOM ACCESS MEMORY

FOLD OUT SCHEMATIC SHEETS 3 AND 4, PAGES 75 AND 76, FOR EASY REFERENCE.

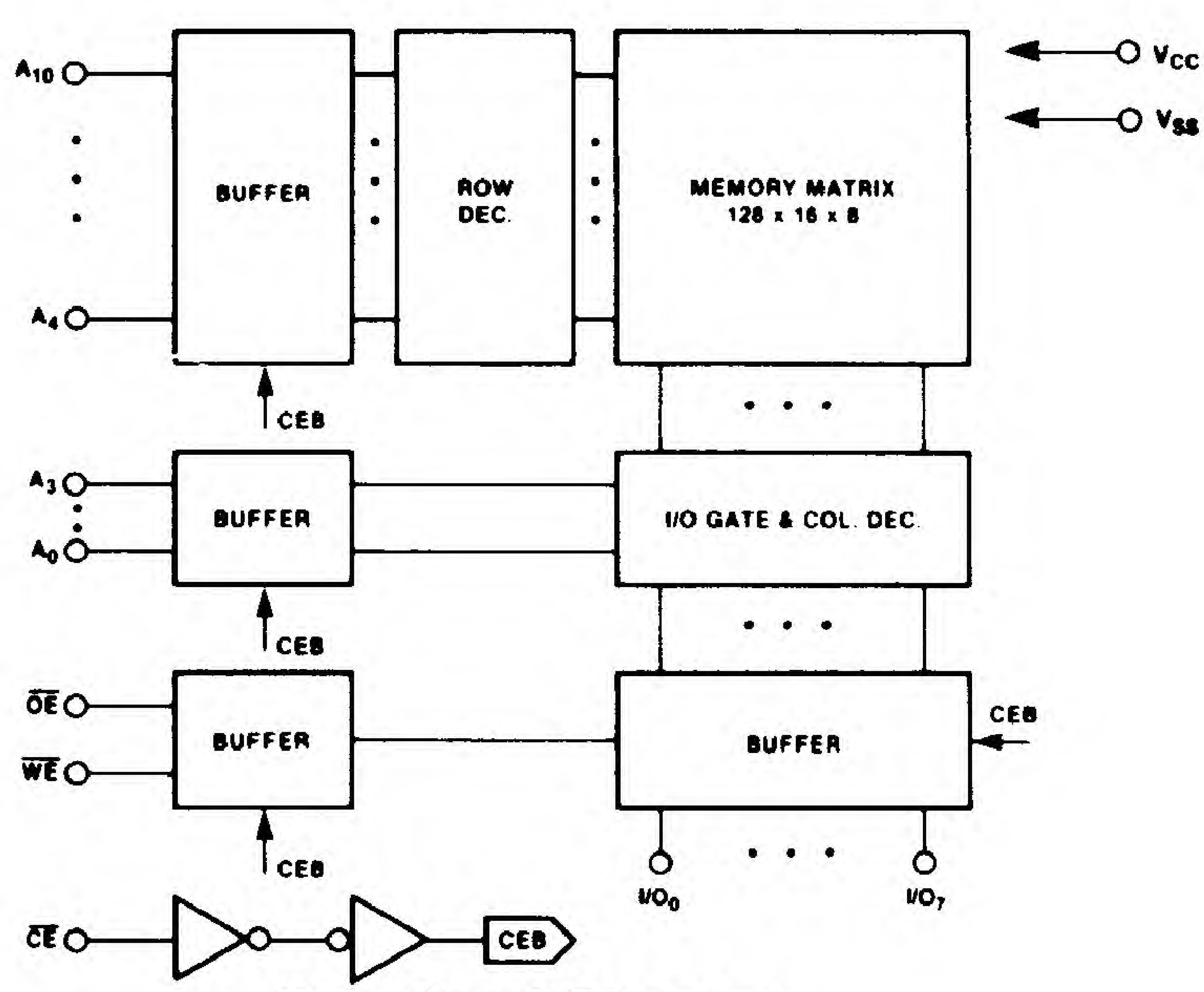
The C128 System contains 128K of processor-addressable 4164 DRAMs in the 64K x 1 configuration, organized into two individual 64K banks. Additionally, the system contains 16K of video display 4416 DRAMs (16K x 4) local to the 8563 CRT Controller, and 8K of STATIC RAM used as VIC COLOR RAM.

RAM banking, described in detail in the MMU section, is controlled by several MMU registers: the Configuration Register, the RAM Configuration Register, and the Page Zero and Page One Pointers. Simply put, the Configuration register controls which 64K bank of RAM is selected, the RAM Configuration Register controls if and how much RAM is kept in common between banks, and the Pointer registers redirect the zero and one pages to any page in memory, overriding the effect of the two configuration registers. In the system, RAM bank select is achieved via gated CAS control.

2016
2K x 8 STATIC RAM

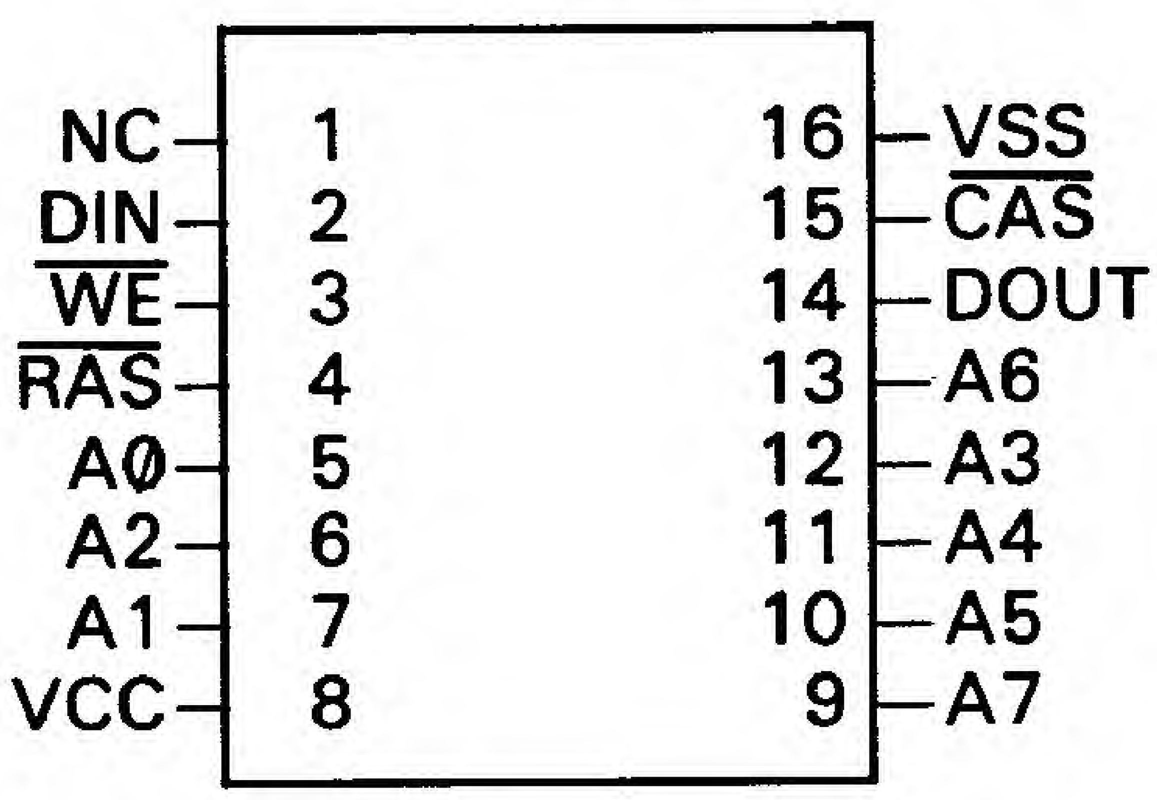


1-8, 19, 22 23	A_0-A_{10}	Address Bus Inputs.
9-11, 13-17	I/O_0-I/O_7	Common Data Input/Output Lines.
12	V_{SS}	Ground.
18	CS	Chip Select Enable, Low Active.
20	OE	Output Enable, Low Active.
21	WE	Write (Input) Enable, Low Active.
24	V_{CC}	5VDC Input.

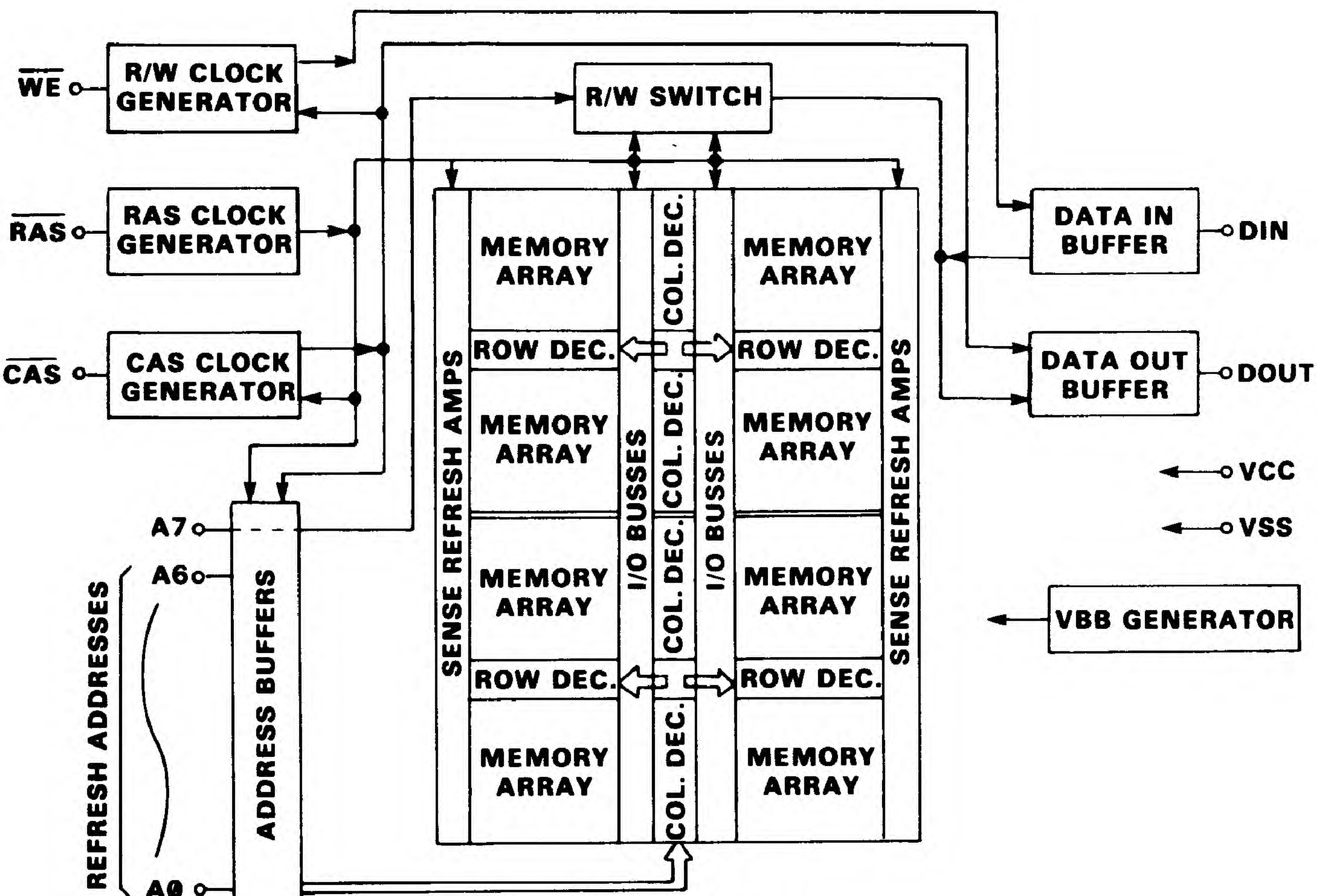


Functional Diagram

4164
64K x 1 DYNAMIC RAM

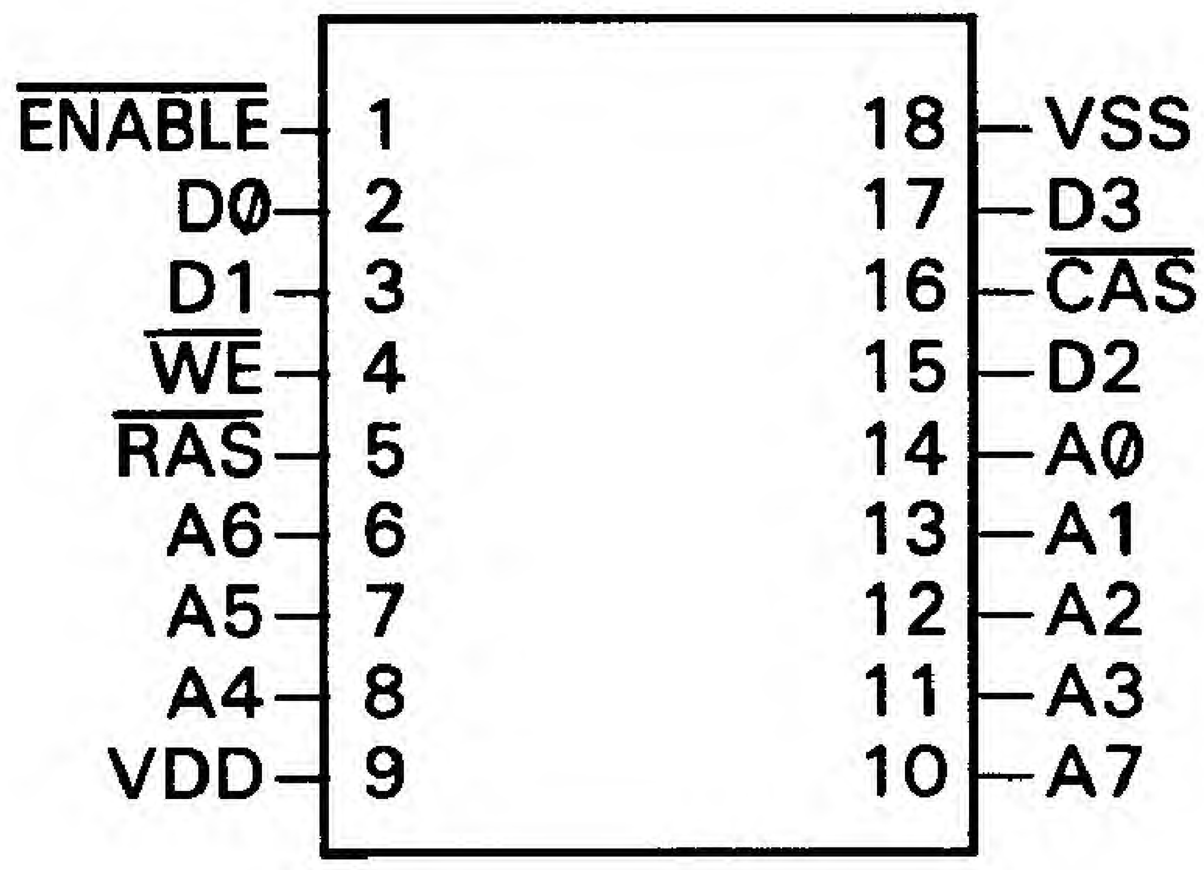


1	NC	Unused.
2	DIN	Data Input.
3	WE	Write Enable. Low active control input.
4	RAS	Row Address Strobe Input. Low active.
5-7, 9-13	A0-A7	Address Bus Inputs.
8	VCC	5VDC Input.
14	DOUT	Data Output.
15	CAS	Column Address Strobe Input. Low active.
16	VSS	Ground.

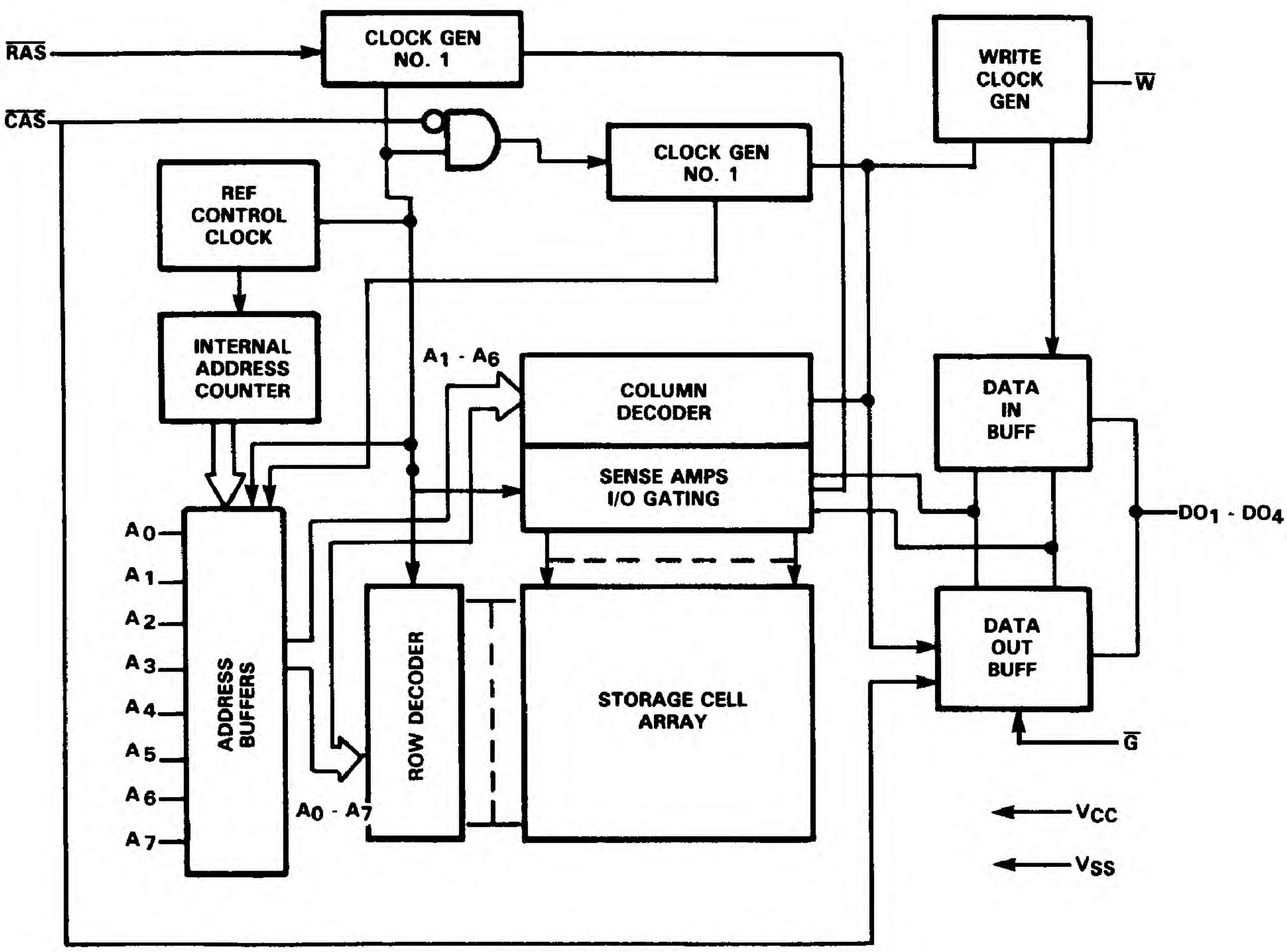


Functional Diagram

4416
16K x 4 DYNAMIC RAM



1	ENABLE	Output Enable ($\overline{G}$).
2,3, 15,17	D0-D3	Common Data Input/Output Lines.
4	WE	Write (Input) Enable. Low Active.
5	RAS	Refresh Address. Low Active.
6-8, 10-14	A0-A7	Address Bus Inputs.
9	VDD	5VDC Input.
16	CAS	Column Address Strobe. Low Active.
18	VSS	Ground.



Functional Diagram

THE MEMORY MANAGEMENT UNIT

FOLD OUT SCHEMATIC SHEET 2, PAGE 74, FOR EASY REFERENCE.

The MMU is designed to allow complex control of the C128 system memory resources. It handles all of the standard **C64 modes of** operation in a fashion as to be completely compatible with the C64. Additionally, it controls the management of particular C128 modes including the Z-80 mode.

Summary of MMU functions:

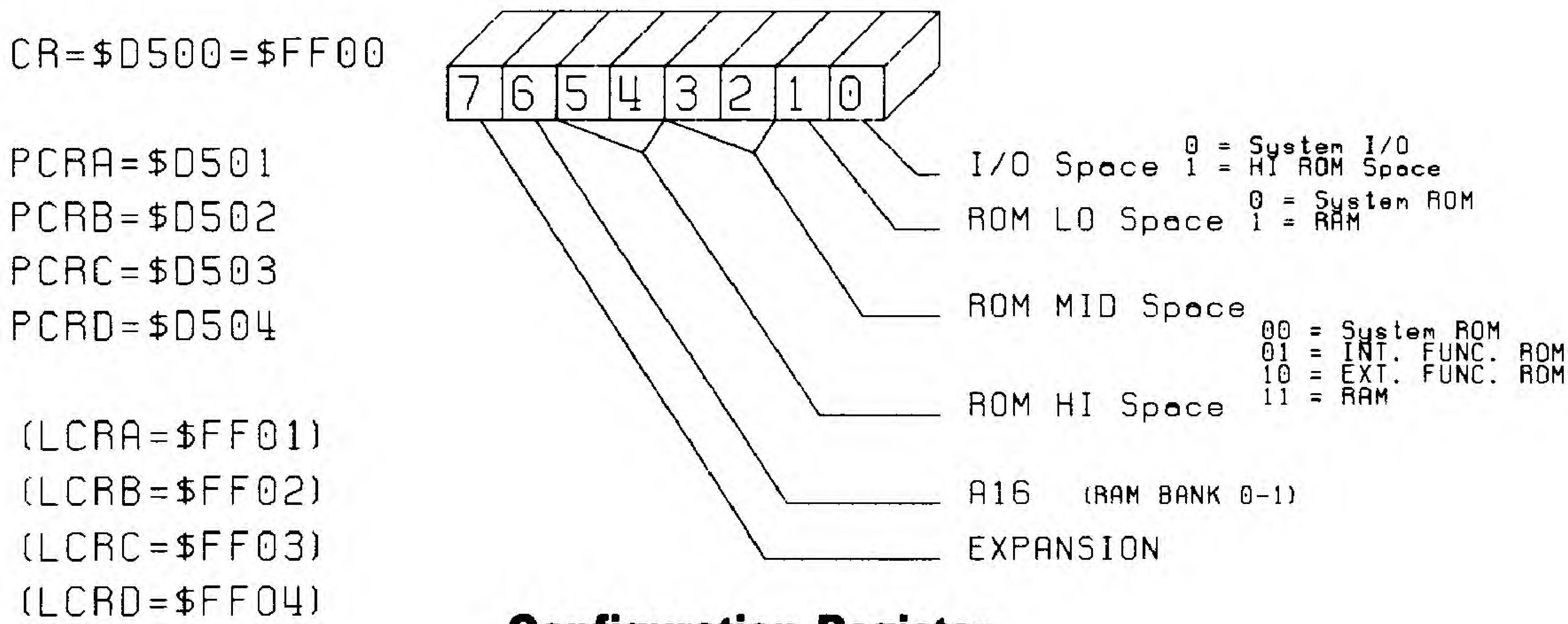
- Generation of Translated Address Bus, $TA_8 - TA_{15}$.
- Generation of control signals for different processor modes — C128, C64, Z-80.
- Generation of CAS select lines for RAM banking.
- Generation of ROMBANK (MS_0, MS_1) lines for ROM banking.

The MMU is the mechanism by which the various memory modes shown in the C128 Memory Map are chosen. Additionally, the MMU provides for Z-80 mode, which was not shown on that diagram. Following is a description of the MMU register types. Note that in C64 mode the MMU completely disappears from the system's memory map. Note that the data out of the MMU is valid **only** on AEC high. This is necessary to avoid bus contention during a VIC cycle.

$FF04	LCRD	LOAD CONFIGURATION REG D
$FF03	LCRC	LOAD CONFIGURATION REG C
$FF02	LCRB	LOAD CONFIGURATION REG B
$FF01	LCRA	LOAD CONFIGURATION REG A
$FF00	CR	CONFIGURATION REGISTER

$D50B	VR	VERSION REGISTER
$D50A	P1H	PAGE 1 POINTER HIGH
$D509	P1L	PAGE 1 POINTER LOW
$D508	P0H	PAGE 0 POINTER HIGH
$D507	P0L	PAGE 0 POINTER LOW
$D506	RCR	RAM CONFIGURATION REGISTER
$D505	MCR	MODE CONFIGURATION REGISTER
$D504	PCRD	PRECONFIGURATION REGISTER D
$D503	PCRC	PRECONFIGURATION REGISTER C
$D502	PCRB	PRECONFIGURATION REGISTER B
$D501	PCRA	PRECONFIGURATION REGISTER A
$D500	CR	CONFIGURATION REGISTER

MMU Register Map



Configuration Register
Preconfiguration Register

The Configuration Register

The **Configuration Register**, CR, controls the ROM, RAM, and I/O configuration of the C128 system. It is located at $D500 in I/O space and at $FF00 in system space. Some of the bits in this register are at times reflected by hardware lines MS_0 and MS_1 in C128 mode, depending upon how RAM and ROM have been set. These MS lines are used to inform the PLA about the type of memory in a particular address range. In C64 mode, MS_0 and MS_1 are always high, and the selection of RAM and ROM is done by the PLA using standard C64 banking methods. The MS lines are alternately referred to as ROMBANK lines. They will be referred to as MS lines in this section in the interest of simplicity.

In C128 mode, bit 0 controls whether an I/O space, $D000 — $DFFF, or a ROM/RAM access occurs. A low will select I/O, a high will enable some kind of ROM/RAM access, the nature of which is controlled by other bits in this register. The value of this bit is stored in a prelatch, until the fall of the clock, in order to prevent its changing in an unstable situation. Note that when not I/O space, the ROM/RAM access is controlled by the defined ROM Hi configuration bits, which are described later. This bit resets to 0. When the I/O bit is low, MMU registers $D500 to $D50B will assert themselves. When the bit is high, these registers disappear from the memory map. MMU registers $FF00 to $FF04 are always available in C128 mode. The hardware line I/OSE always reflects the polarity of this bit when in C128 mode. In C64 mode the I/OSE line, the hardware line driven by this bit, is completely ignored by the PLA, and the MMU is never asserted, even when C64 I/O is enabled. The C64 method of selecting I/O via HIROM and CHAREN takes over here. The I/O hardware line remains in its set state when in C128 mode, even though it has no effect in this mode.

Bit number 1 controls processor access to ROM low space, $4000 — $7FFF, in C128 mode. If the bit is high, the area will appear as RAM, and a RAM access, CAS enable, will be generated to the appropriate RAM bank, which is determined by other bits in this register. If low, system ROM will be located in the space. This bit affects the memory status lines MS_0 and MS_1 which are decoded by the PLA to generate ROM chip selects. Selecting ROM here will drive both memory status lines low when the processor address falls within the specified low space range. This bit resets low to include the C128 Basic Low ROM. Of course in C64 mode, this bit is ignored.

The next two bits, bits 2 and 3, determine for C128 mode the type of memory that will be located in the mid space, $8000 — $BFFF. If they are both low, system ROM will be located here. If bit 2 alone is high, internal function ROM is located here. External function ROM appears for bit 3 being alone high, and RAM appears, along with the proper CAS generation, for both bits set high. These bits also affect the hardware memory access lines. When in the aforementioned mid block address range, MS_0 will reflect the status of bit 3, and MS_1 will reflect the status of bit 2. These bits both reset low to start out with Basic Hi. C64 mode ignores these bits.

Bits 4 and 5 determine the contents of the Hi block, $C000 — $FFFF, for C128 mode, and have no effect on C64 mode. As with the mid space, both bits zero will set up system ROM, bit 4 high will set up internal function ROM, bit 5 high will set up external function ROM, and both bits high will set up RAM. Note that the I/O configuration bit, when set for I/O space, will leave the area from $D000 to $DFFF as I/O space, regardless of the values of these bits. If not set for I/O space, $D000 to $DFFF will contain the character ROM if the ROM chosen is System ROM. As with the other ROM selection bits, these bits are reflected by the memory status lines when this region of address is accessed. Bit 5 corresponds to MS_0 and bit 4 to MS_1. Both of these bits reset to low to permit Kernal and Character ROM to power up in this address space. Note that there is always a hole in high ROM during C128 mode for the MMU registers at $FF00 to $FF04. This hole is brought about by holding both MS lines high and both CAS enable lines high. These bits are ignored in C64 mode.

Finally, bit 6 controls the RAM bank selection. When low, it will select bank 0 by dropping CAS_0. When high, it will select bank 1 by dropping CAS_1. Bit 7 is unassigned at the present, left for future expansion. Note that a RAM share status that is non-zero will override the normal CAS enable generation to provide CAS_0 for all shared memory. Also, note that when the proper CAS enable is generated, any area of memory, even if that area does not have its ROM bank bits set for RAM, is accessed. It is up to the PLA to block CAS for a read from ROM. This allows RAM bleed through on a write to ROM. For any access to the MMU registers from $FF00 to $FF04, in any C128 mode configuration, both CAS enable lines and both MS lines will be high. Note that in C64 mode, the bank used follows the same rules as in C128 mode, though of course banks cannot be changed once in C64 mode.

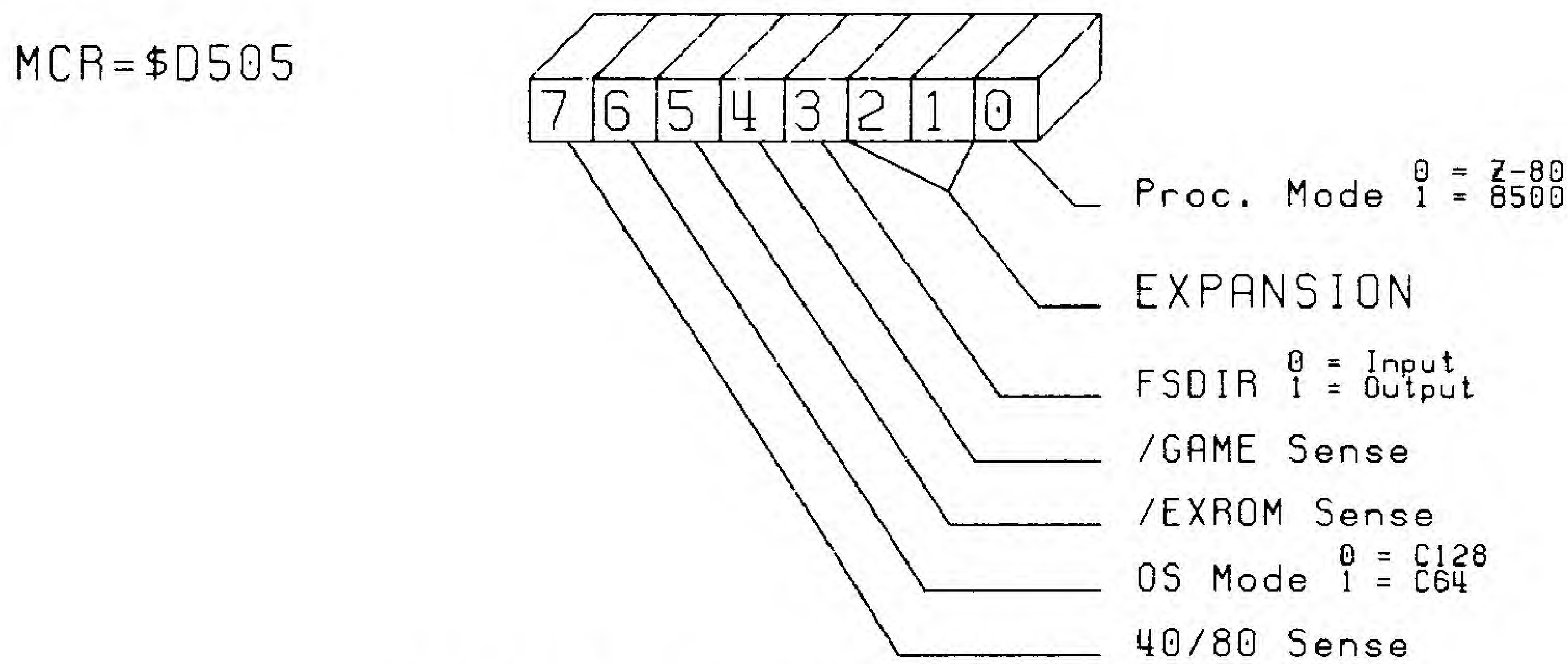
The Preconfiguration Mechanism

The Preconfiguration Mechanism is a feature of the MMU that allows the Configuration Register to be loaded with one of several memory configurations, with a minimum of time and memory on the part of the user. The scheme makes use of two sets of registers, the **Preconfiguration Registers** and the **Load Configuration Registers.**

The Preconfiguration Registers (PCRA — PCRD) are used to store several different memory configurations that may be accessed with a single store instruction. The format of each preconfiguration register is the same as for the Configuration Register but, when a value is stored to a preconfiguration register, no immediate effect takes place. They occupy I/O space from $D501 to $D504. These registers always reset to all zeros.

Load Configuration Registers (LCRA — LCRD) directly correspond with the preconfiguration registers on a one-to-one basis. A write to a Load Configuration Register causes the contents of the corresponding Preconfiguration Register to be transferred to the Configuration Register. A read of any Load Configuration Register returns the value of its corresponding Preconfiguration Register. Load Configuration Registers are located in system space from $FF01 to $FF04. Neither the Load Configuration Registers nor the Preconfiguration Registers have any effect in C64 mode. These registers reset to all zeros. Note that these, and the configuration register at $FF00, will **always** be available, completely independent of the ROM, RAM, or bank configuration defined for Hi ROM space. Any address in this range will cause the MMU to force both memory status lines and both CAS enable lines high.

THE MEMORY MANAGEMENT UNIT (Continued)



Mode Configuration Register

The Mode Configuration Register

The control of the current system mode is governed by the **Mode Configuration Register**, MCR. It controls which processor, 8502 or Z-80, and which operating system mode, C64 or C128, is currently in operation, and handles other overhead of the different operating modes. This register is located in the I/O space at $D505.

Several of the bits in this register function as bidirectional ports, including the FSDIR, GAME, EXROM, and 40/80 bits. This type of port functions like an output port. If a value is written to the port, its hardware line will reflect that value written, and a read will return that value. The only exception to this is if an external source is pulling down the corresponding port line. When pulled down, a read of the port will return a low. Once the external source has been removed, a read will return the value previously stored. Thus, as an input, the port can be driven low, but not high, by an external source. Under each bit description, both the input and output functions of each port bit will be described in detail.

The first bit, bit 0, controls which processor is enabled. It is reflected by the output line **Z80EN**. When low, it indicates that the processor is the Z-80. This is the reset configuration, and will cause the Z-80 processor to be active and all accesses to memory to follow the Z-80 mapping rules. In Z-80 mode, any address to RAM bank 0 in the range from $0000 to $0FFF will be translated to the corresponding address in the range from $D000 to $DFFF, where the Z-80 CP/M BIOS physically exists in System ROM. Additionally, the memory status lines MS_0 and MS_1, will reflect system ROM (both low) for accesses in the range of the BIOS, and the page zero and page one offset pointers will be disabled. RAM can still be banked by the CR A_{16} bit, which controls CAS_0 and CAS_1. When in bank one, the BIOS ROM disappears, allowing the RAM from $0000 to $FFFF to be used by the system, and enabling the page zero and one offset pointers.

A change to this processor select bit is held in prelatch until a clock transition, in order to prevent processor changing in the midst of an instruction execution. Bringing this bit high will cause the Z-80 to be disabled and the 8502 to take over. Upon system power up, the Z-80 will turn itself off and bring up C128 mode by setting this bit and allowing the 8502 to take over.

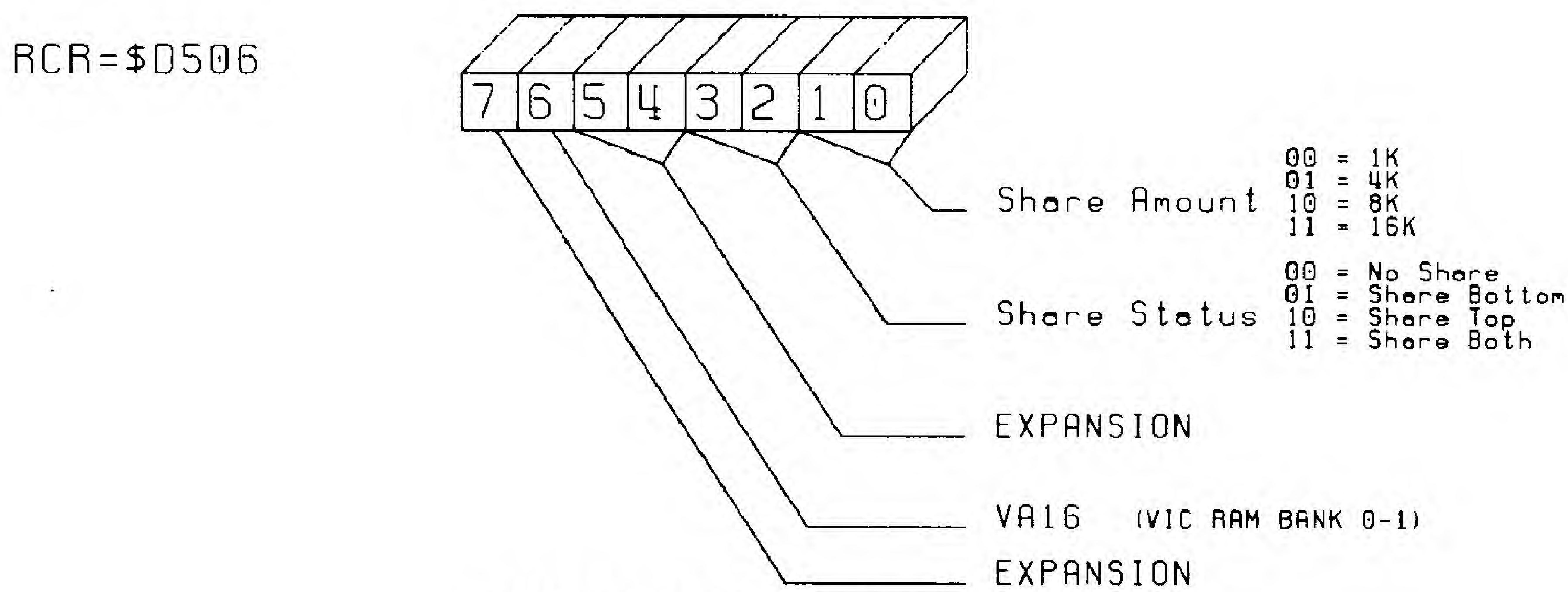
Bits 1 and 2 are unused, but are reserved for future expansion as possible port lines. Currently, they will return high if read, and cannot be written to.

Bit 3 is the **FSDIR** control bit. It is used as an output to control the fast serial disk data direction buffer hardware, and as an input to sense a fast disk enable signal. This bit is a bidirectional port bit as explained above, and its hardware line is called **FSDIR**.

Bits 4 and 5 are the $\overline{GAME}$ and $\overline{EXROM}$ sense bits, respectively, which are implemented as bidirectional ports as explained above. As inputs, they directly reflect the hardware cartridge control lines $\overline{GAME}$ and $\overline{EXROM}$ as used in C64 mode. C128 cartridges do not use $\overline{EXROM}$ and $\overline{GAME}$, so if they are detected in C128 mode, a C64 cartridge is present and C64 mode should be asserted. They have no dedicated C128 function.

The operating system mode is set by bit 6. This bit is cleared to zero upon reset and its presence enables all MMU registers and other C128 features, as well as asserting the C128 control line in hardware. Setting this bit removes the MMU from the memory map and sets the system up in C64 mode. Note that the C128 MS_3 hardware line reflects a logical inversion of the level of this bit.

Bit 7 is used to detect the status of the screen mode switch, as presented in hardware to the Sense40 column pin. If this bit is high, the 40/80 column switch is open, if low, the switch is closed. The display mode will be set according to a software interpretation of this bit. This bit is a bidirectional port bit, but its output function is undedicated at this time.



RAM Configuration Register

The RAM Configuration Register

The **RAM Configuration Register** sets up the RAM segmenting parameters for both the processor and the block pointer for the VIC chip. This register is located in the I/O space at $D506.

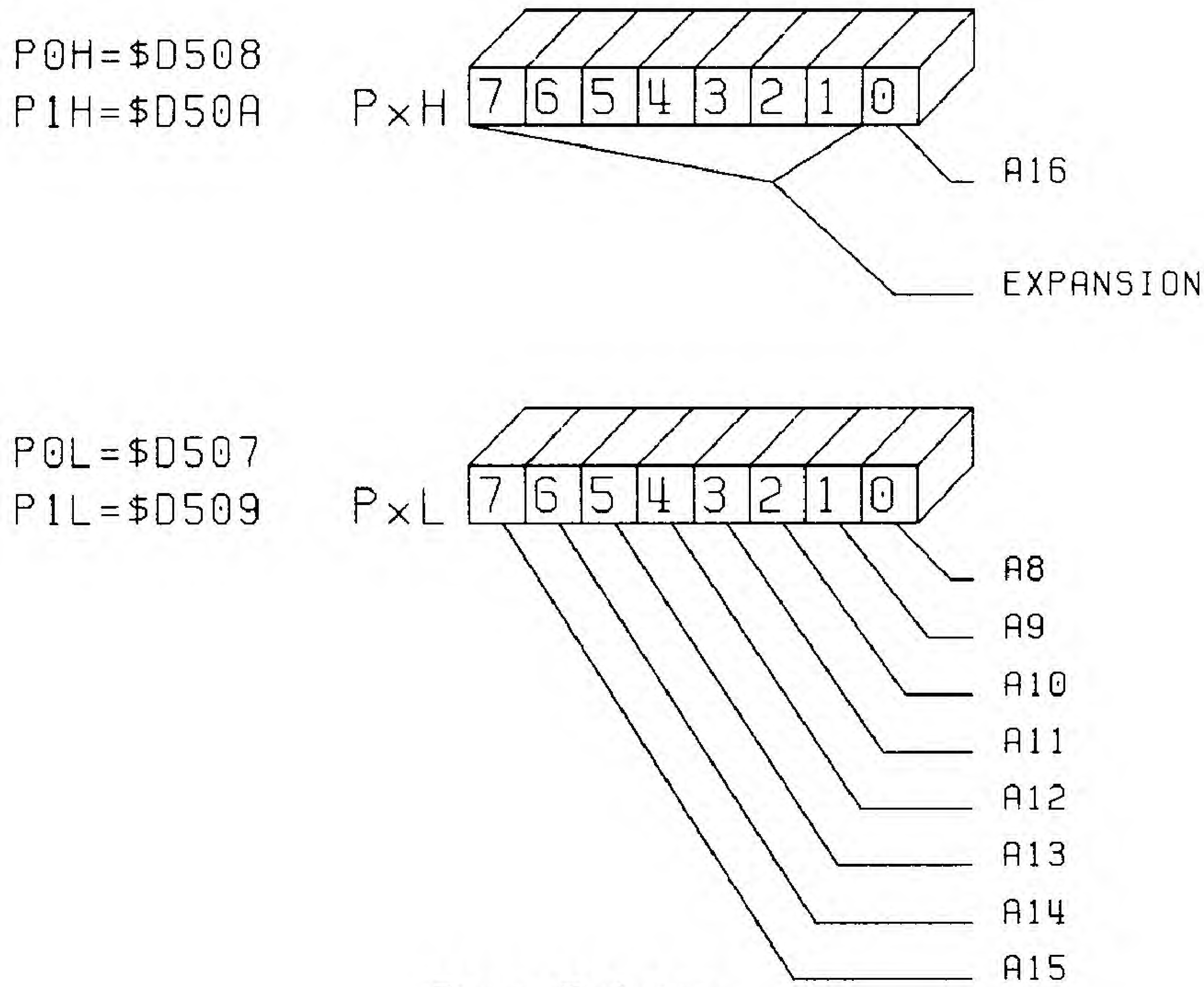
Bits 0 and 1 function together to determine the size of the RAM to be shared between banks, assuming that sharing is enabled. With common RAM, the RAM bank bits of the configuration register are basically overridden, as the selected bank of RAM will be used for the non-common areas, while bank 0 will be used for the specified common areas. ROM and I/O block configuration bits, however, are still important. If the value of the bits together is 0, then 1K of RAM is held common. If the value is 1, then 4K; 2, then 8K; 3, then 16K. These bits have no effect in C64 mode, and the reset value of both bits is defined to be zero.

Bits 2 and 3 function to determine how and if RAM is kept common. If both are low, no sharing takes place. If bit 2 is set, the bottom RAM is shared. If bit 3 is set, the top RAM is shared. Both may be set at the same time for sharing both top and bottom memory. The reset configuration sets both of these bits zero, such that no common memory is present.

The next two bits, numbers 4 and 5, are not used in this MMU. They are available for possible future expansion. They read low, and cannot be written to.

Bit 6 functions as a RAM bank pointer for VIC. It is used to drive CAS_0 low when set low or CAS_1 low when set high, thus selecting either RAM bank 0 or RAM bank 1 for the VIC, independently from the processor bank. When in 2 MHz mode the 80-column chip takes over, causing the VIC to be disabled. This disabling is affected by the VIC chip itself holding AEC constantly high, and thus is not directly effected by actions of the MMU. Note that since a VIC cycle is detected by AEC low, that any DMA will put the MMU into VIC configuration, as it too brings AEC low. This allows independent bank selection for DMAs in 80 column mode.

Bit 7 is currently unused.



Page Pointer

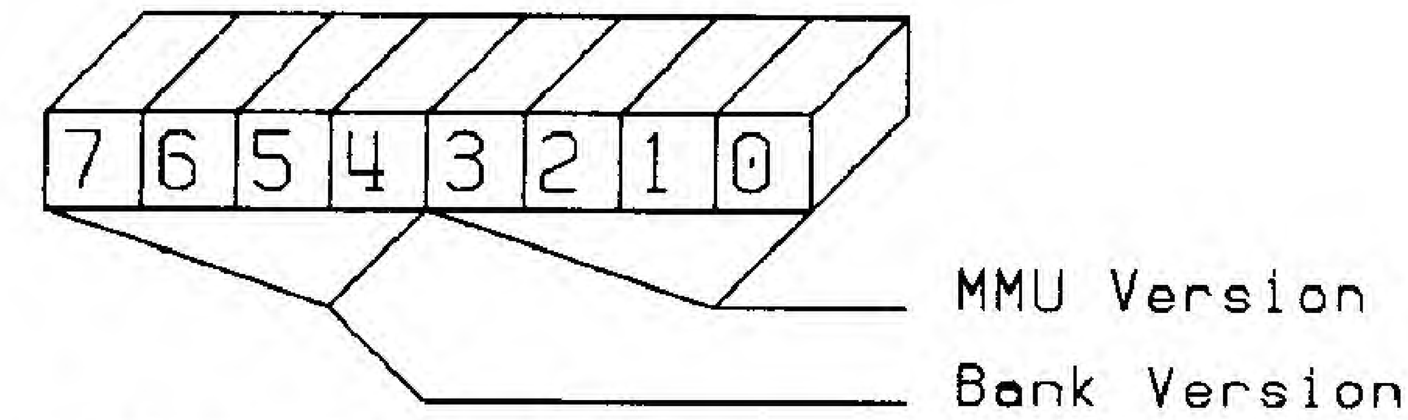
The Page Pointers

The page pointers are four registers that allow independent relocation of pages zero and one, when running under either processor. These are especially useful when running under the 8502 as they help to remove some of the zero page and stack size limitations normally associated with 6502 family processors.

For zero page relocation, the MMU provides the **Page Zero Pointer High** ($P0_H$) and **Page Zero Pointer Low** ($P0_L$) registers. Bit 0 of the $P0_H$ register corresponds to translated addresses TA_{16} for any zero page access, $0000 — $00FF, controlling the generation of CAS_0 or CAS_1 depending on whether it is low or high. The remaining bits are currently unused, and will always return zero. These bits override the RAM bank bits, the ROM block, and the I/O block bits to determine which physical page appears as zero page for all zero page accesses. A write to the $P0_H$ register is stored in prelatch until a write to the $P0_L$ register occurs. Bits 0 to 7 of the $P0_L$ correspond to Translated Addresses TA_8 to TA_{15} for any zero page access, thus relocating the zero page. Any access to the area that has become the relocated zero page will be switched back to the original zero page if that area is mapped as RAM. If mapped as ROM, then the reverse mapping is not done, allowing access to the ROM. A write to this register sets up the zero page transfer, which can occur as soon as the next low clock cycle. Register $P0_L$ is located in the I/O space at $D507, while register $P0_H$ is located at $D508.

The registers for page one relocation, the **Page One Pointer High** ($P1_H$) and the **Page One Pointer Low** ($P1_L$) do for page one essentially what $P0_H$ and $P0_L$ do for the zero page. The functions and bit correspondences are exactly the same. $P1_L$ is located in the I/O space at $D509 and $P1_H$ at $D50A. Note that both register pairs are initialized upon reset to reflect true page zero and true page one access for the 8502 processor. Note that these registers continue to take effect in Z-80 mode, as well as in 8502 mode, when set to bank one. When set to bank zero, they are disabled to provide true Z-80 BIOS access.

VR=$D50B

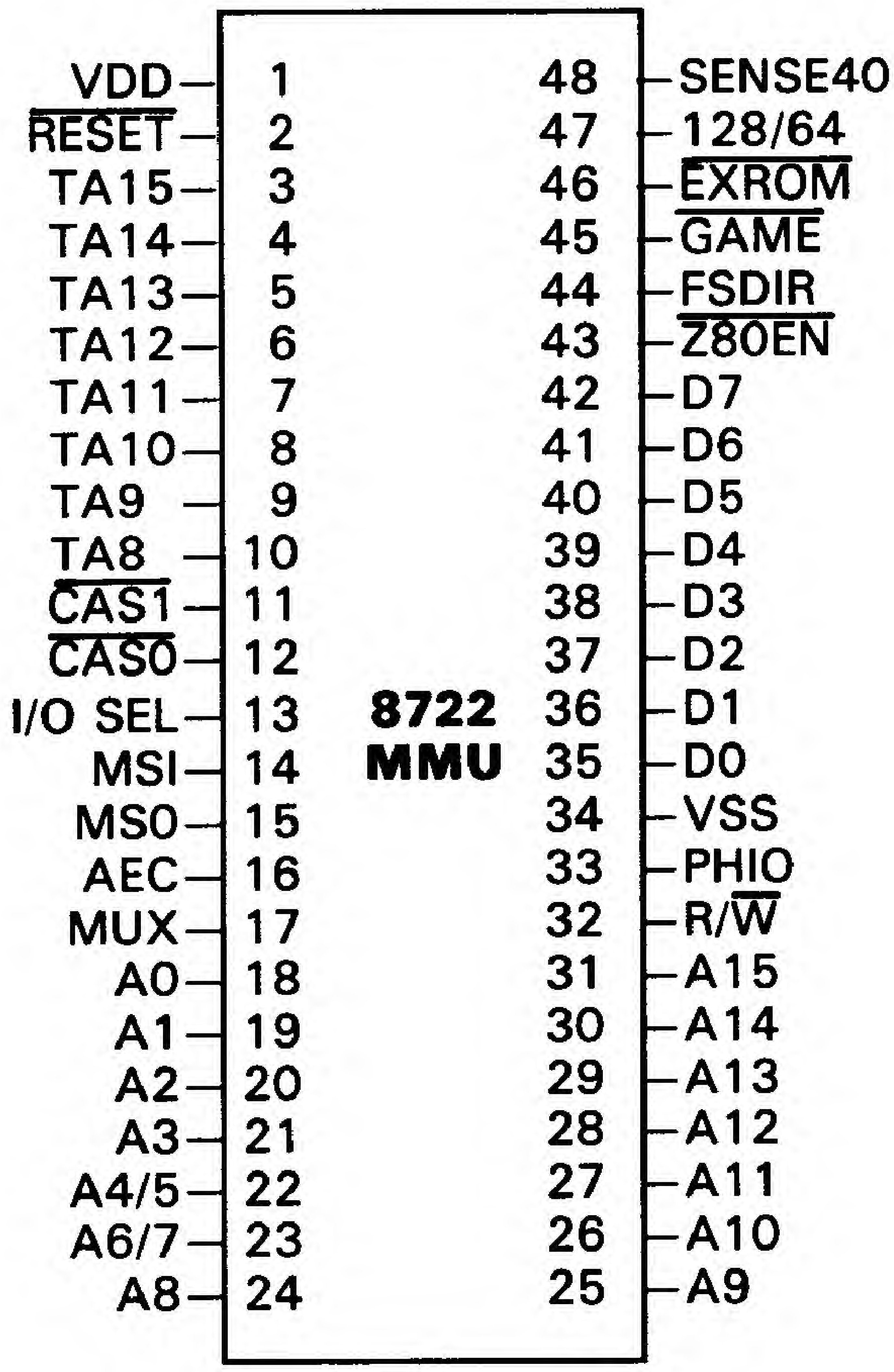


Version Register

System Version Register

The final register is the **System Version Register,** which is located at $D50B in the I/O block. This register is a read-only register that returns a code containing the version of the MMU and the size and capability of the system's memory. The lower nybble, bits 0 through 3, contain the version of the MMU in the system. The upper nybble, bits 4 through 7, contains a code relating the number of memory blocks available in the system. This allows software to compensate for any later systems with more available memory, and should make it quite simple for the current C128 to remain compatible with any software written in the future for an expanded C256, etc. system. The initial C128 will read a 2 here, indicating two 64K blocks are available. A zero in this nybble would indicate sixteen 64K blocks.

310389
8722 MEMORY MANAGEMENT UNIT



1	VDD	5VDC input.
2	RESET	System Reset. This input initializes internal registers on a power up or hardware reset.
3-10	TA8-TA15	Translated Address outputs. Tri-stated for VIC cycles during AEC, provides translated physical address for use on the Multiplexed Address Bus and the Shared Static Bus. TA_{12} to TA_{15} are each defined to have an internal, depletion mode pullup with an equivalent resistance of 3.3KΩ. TA_8 to TA_{11} each go tristate during VIC time (AEC low).
11,12	CAS_0, CAS_1	Column Address Strobe. The CAS output lines control DRAM banking. CAS_0 enables the first bank of 64K, CAS_1 enables the second bank of 64K.
13	I/O SEL, MS_2	I/O Select, Memory Status 2. This output is identified by both identifiers. It is used to select memory mapped I/O in C128 mode and is also know as MS_2. In C128 mode, this line always reflects the polarity of the I/O bit. It is ignored by the PLA in C64 mode, and remains high throughout C64 mode.
14,15	MS_0, MS_1	Memory Status 0, 1. Also called $ROMBANK_0$ and $ROMBANK_1$, these outputs control ROM banking for all ROM slots. These lines are used to decode ROM bank selection for any ROM access in C128 mode. If they are both low, a system ROM has been selected. If MS_1 is high alone, then a built in function ROM has been selected. If MS_0 is alone high, then an external function ROM has been selected. Finally, if both are high, the RAM that occupies the particular slot has been selected. In C64 mode the PLA completely ignores these lines.
16	AEC	The Address Enable Control indicates whether the 8502 processor or the VIC has access to the shared bus. When low, VIC or an external DMA has the bus and VA_{16} and VA_{17} have the processor bus, and no pointer or BIOS translation takes place.
17	MUX	The Memory Multiplex signal, used to clock various sections of the MMU.
18-31	A0-A15	A0 - A3, A8 - A15: Addresses from the microprocessor. Used to derive chip selects as well as multiplexed address lines. A4/5, A6/7: Combined addresses from the microprocessor. Used along with simple addresses, combined in this fashion to lower the pin count of the MMU.
32	R/W	R/W: System Read/Write control line. This input is high for a processor read, low for a processor write.
33	PHI_0	Presystem clock. Used for early transition of gated signals on write operations. Processor address is valid on the rising edge and data is valid on the falling edge.
34	VSS	System Ground.
35-42	D_0-D_7	Data inputs from the microprocessor. Used for writing to internal registers.
43	Z80EN	This output is used to enable the Z80 processor and disable the normal operation of the 8502 processor. It goes low to indicate Z-80 mode, high for all other modes.
44	FSDIR	Fast Serial Direction. This port is a bidirectional line that in output mode controls the data direction of the fast serial disk interface.
45	GAME	Game ROM Enable. This signal is used to sense the GAME line on the expansion connector in C64 mode and as the color RAM bank control line in C128 mode.
46	EXROM	External ROM Enable. This signal is used to sense the EXROM line on the expansion connector in C64 mode and as an expansion control line in C128 mode.
47	128/64, MS_3	This output directs the system to act in either C128 or C64 mode. It goes low to indicate C64 mode, high for C128 mode.
48	40/80	Sense 40/80. This bidirectional port is used in input mode to sense the 40/80 column switch. It detects whether or not the switch is closed. The output mode is not used at this time.

THE PROGRAMMED LOGIC ARRAY

FOLD OUT SCHEMATIC SHEET 2, PAGE 74, FOR EASY REFERENCE.

The 8721 C128 PLA is a programmed version of the Commodore 48 Pin Programmable Logic Array. It provides all of the chip selects and other decoded signals that were necessary for the C64, along with a number of such signals new in the C128 system.

Summary of PLA functions:

- Control all ROM selects (KERNAL, BASIC, FUNCTION, EXTERNAL) in all operating modes.
- VIC chip select.
- Color RAM chip select.
- Character RAM chip select.
- Gated write enable to color RAM.
- Latched write enable to DRAMs.
- Z-80 select decoding.
- Z-80, I/O decoding, for Z-80 I/O cycle and Z-80 memory mapping.
- Data bus direction signal.
- I/O group chip select (includes I/O-1, I/O-2, CIA-1, CIA-2, SID, 8563).
- I/O access signal indicating an I/O operation is occuring.
- Column Address Strobe Enable for DRAM.

Chip Select Generation

The PLA device is responsible for defining the banking rules for ROM and RAM that the system will follow. The chip generates chip selects for all ROM and the VIC chip. It generates an enable for any other I/O device in the map, and can enable or disable CAS based upon what else is enabled. In C128 mode, decisions are made using the processor addresses and the four mode status lines: ROMBANKLO, ROMBANKHI, I/O SELECT, and C128/64. The C128 mode banking scheme is quite straightforward and simple. In Z-80 mode, the selection mechanism becomes even simpler, thanks to the I/O cycle of the Z-80 processor.

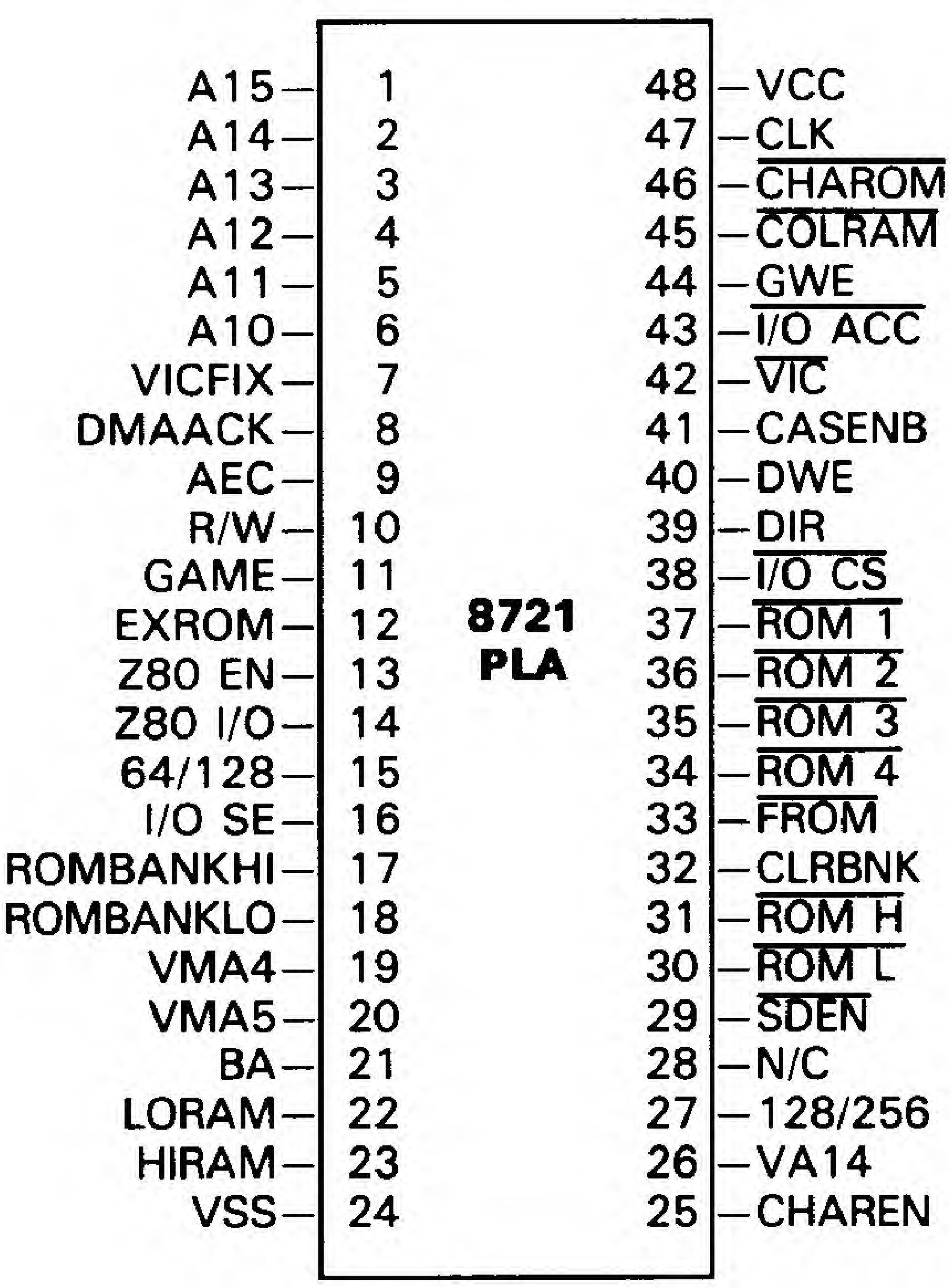
C64 chip selects account for the bulk of the PLA font. The C64 selects I/O, RAM, and ROM based upon the internal control lines BA, HIRAM, LORAM, and CHAREN. The status of these lines, and the decoded addresses, determine for any given time which, if any, chip is selected. When a cartridge is inserted, two additional control lines come into play — $\overline{\text{EXROM}}$ and $\overline{\text{GAME}}$. Various combinations of these lines cause different memory maps to be asserted, all based upon the PLA font.

Other PLA Functions

The PLA performs a variety of functions other than chip selects. It creates the write enable strobes for both DRAM and Color RAM. In C128 mode, the C64 control lines HIRAM, LORAM, and CHAREN are not needed, since the MMU controls the more sophisticated C128 method of banking. Thus, these lines are used to extend the functionality of the C128 at little or no additional cost in hardware. The CHAREN line is used in C128 mode to turn the Character ROM on and off in VIC address space. In the C64, the presence of this ROM was a function of the VIC bank selected. In C128 mode, the ROM can appear or disappear in any VIC bank.

The second of the new functions uses LORAM and HIRAM to select one of two Color RAM banks. The level of LORAM selects the bank that will be seen during processor time, the level of HIRAM selects the bank that will be seen during VIC time. Thus, a program can swap between two full color pictures very clearly, or the processor can modify one full color picture while displaying another.

315012-01 PROGRAMMABLE LOGIC ARRAY

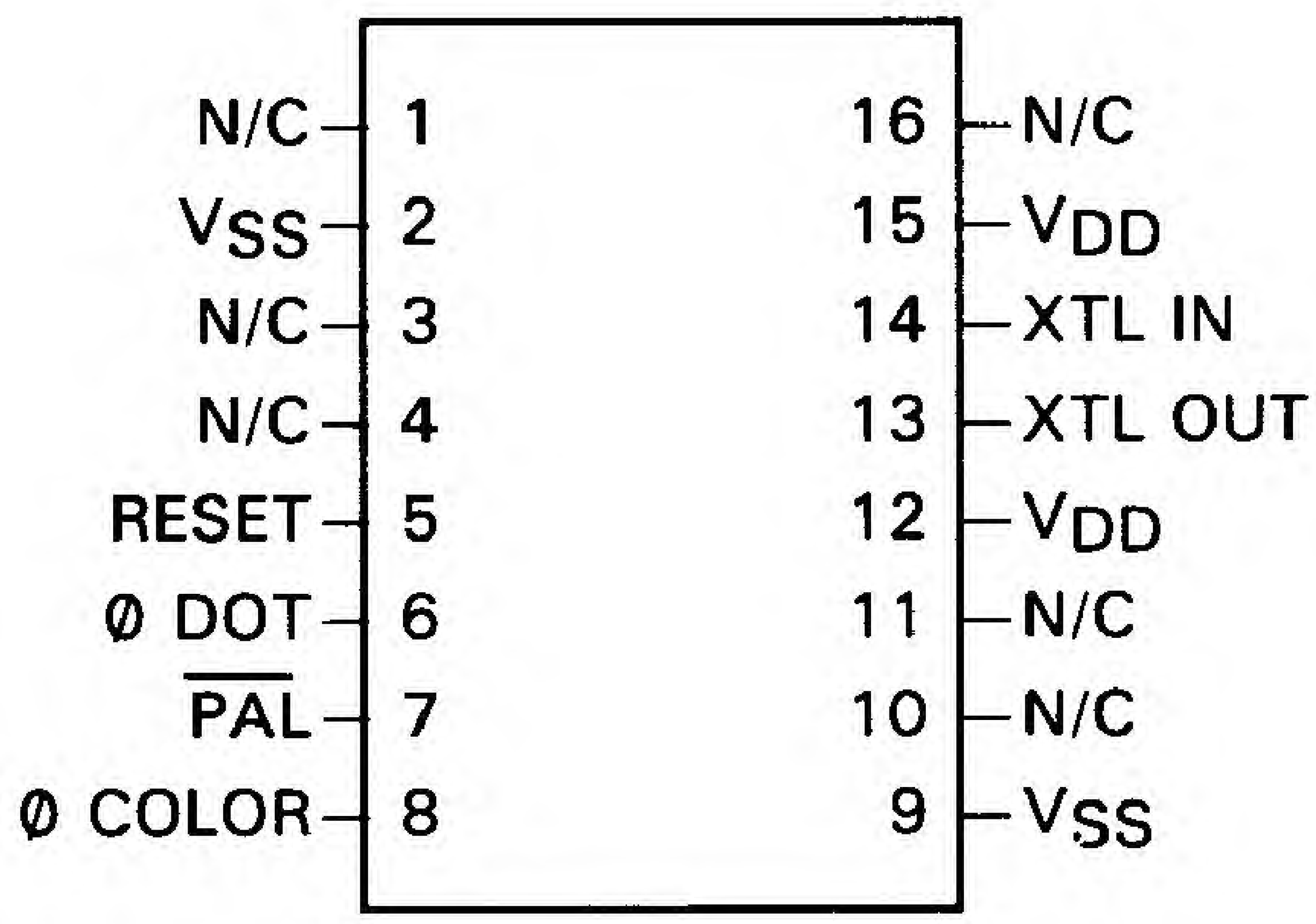


1-6	A_{10}-A_{15}	Address input from 8502 microprocessor.
7	VICFIX	Input to modify CASENB latching for VIC timing.
8	DMAACK	DMA Acknowledge input pulled high in C128 system.
9	AEC	Address Enable Control input from VIC.
10	R/W	Read/Write input from 8502 microprocessor.
11	GAME	Input from the expansion port indicating an external ROM in C64 mode. Unused in C128 mode.
12	EXROM	Input from the expansion port indicating an external ROM in C64 mode. Unused in C128 mode.
13	Z80EN	Input from the Z80 BUSACK line indicating the Z-80 relinquishes the bus.
14	Z80 I/O	Z80 input requesting I/O.
15	64/128	High input sets C128 mode.
16	I/O SE	I/O select input from MMU.
17,18	ROMBANKLO ROMBANKHI	Input from MMU to indicate ROM bank status.
19,20	VMA_4,VMA_5	Input from VIC multiplexed address.
21	BA	Bus Available Input from VIC.
22, 23, 25	LORAM HIRAM CHAREN	Memory configuration signals input from the 8502 port. They are used for C64 mode memory mapping and C128 mode extensions.
24	VSS	Ground
26	VA14	VIC address 14 input from the 6526. Selects video map in C64 mode.
27	128/256	Input line to indicate whether 128K or 256K ROMs are installed in the system. High for 128K, low for 256K.
28	N/C	No connection.
29	SDEN	SD enable output used to enable the buffer between the data bus and the S DATA bus.
30,31	ROM L, ROM H	Active low outputs. They are the chip selects for expansion ROMs.
32	CLRBNK	Output for color RAM bank select.
33	FROM	Function ROM chip select output. Active low.
34-37	ROM 1-4	ROM chip selects for operating system ROM. Active low output.
38	I/O CAS	Active low output used as I/O chip select. Enables external decoder for CIA1 and 2, I/O 1 and SID and 8563.
39	DIR	Data Bus Direction control output for the Data to S Data buffer.
40	DWE	Active low output for DRAM write enable. MUX latches the output in the PLA.
41	CASENB	RAM Column Address Strobe Enable. Used to gate CAS outputs from MMU. The active low output is latched by MUX in the PLA.
42	VIC	Active low output to select the VIC chip.
43	I/O ACC	Indicates access to a 1 MHz part, typically an I/O part. Used by the VIC to stretch the 2 MHz clock.
44	GWE	Active low output used as write enable for color RAM.
45	COLRAM	Color RAM chip select, valid for MPU and VIC.
46	CHAROM	Character ROM chip select, valid for MPU and VIC.
47	CLK	Common clock input from VIC.
48	VCC	5VDC input.

8701 CLOCK GENERATOR

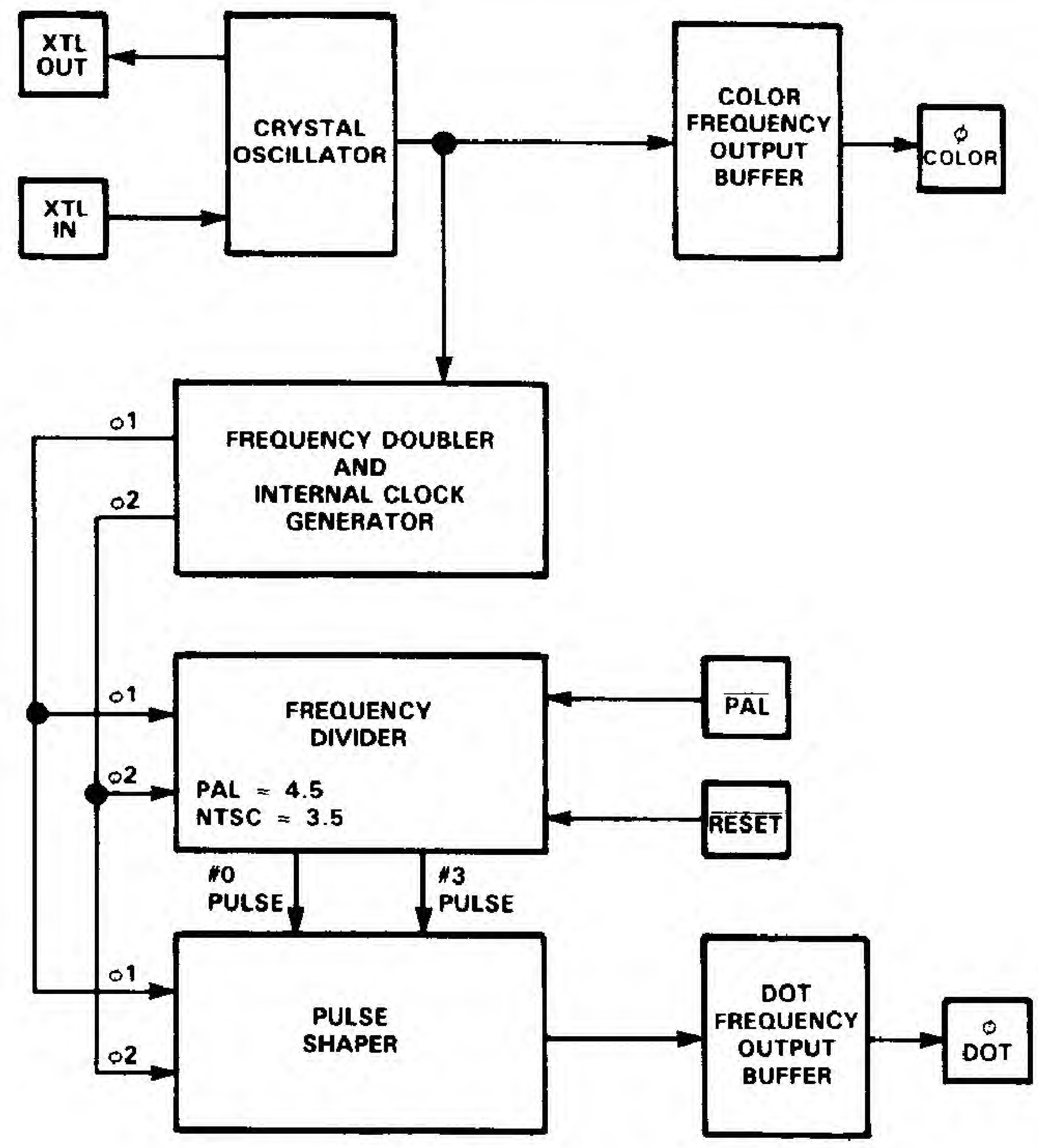
FOLD OUT SCHEMATIC SHEET 3, PAGE 75, FOR EASY REFERENCE.

PIN ASSIGNMENT



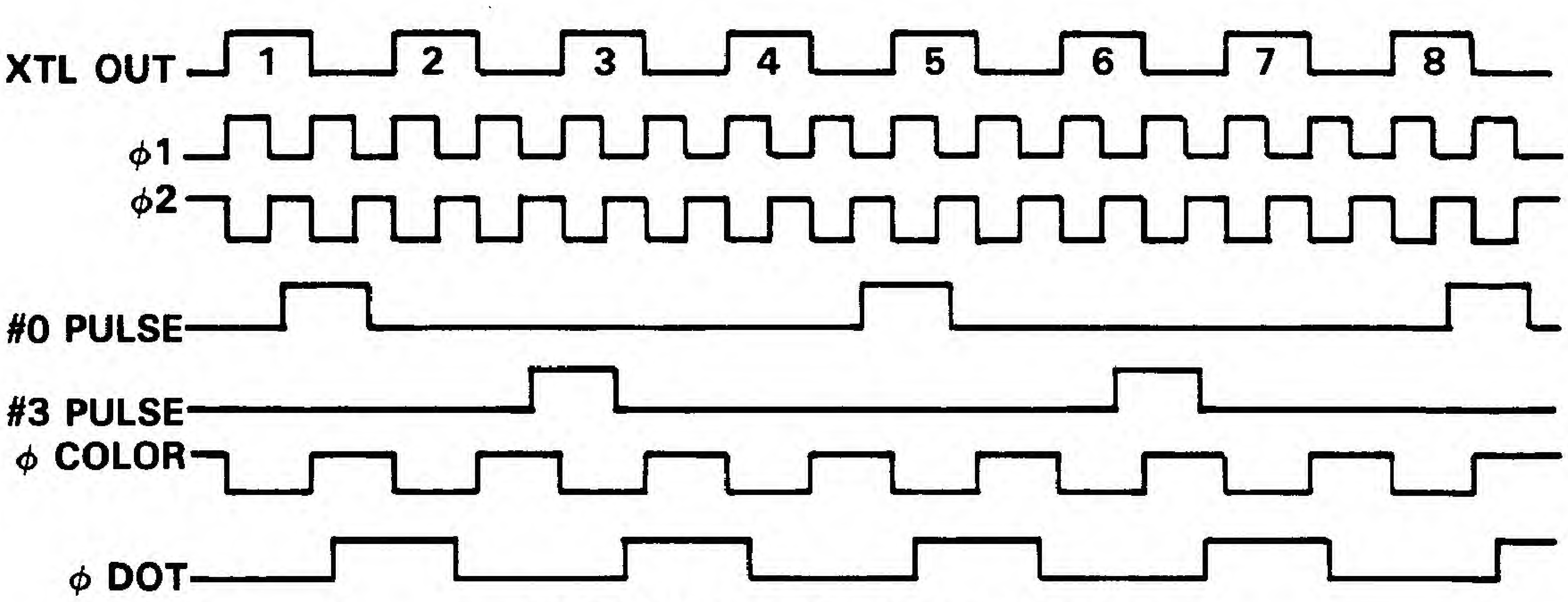
OUTPUTS

Pin 6	Dot Clock	8.1818 MHz.
Pin 8	Color Clock	14.31818 MHz.



Block Diagram

The oscillator circuit uses an external crystal to generate a precise frequency, compatible with either **PAL** or **NTSC** video systems. This frequency can be fine-adjusted using an external trimmer capacitor. The output of this oscillator is buffered and becomes the color clock output. It also goes to the frequency doubler circuit. From there, a pair of non-overlapping clocks are generated (PHI1 and PHI2). These go to the frequency divider which in turn generate a pair of signals, #0 pulse and #3 pulse. Their frequency is determined by the state of the PAL/NTSC input pin. These two pulses go through some digital delays, and with the help of PHI1 and PHI2 are re-combined to form the dot clock frequency. This signal is then buffered and sent out via the dot clock pin.



NTSC Clock Timing Diagram

THE VIDEO INTERFACE

FOLD OUT SCHEMATIC SHEET 3, PAGE 75, FOR EASY REFERENCE.

The C128 VIC video interface hardware allows the connection of a standard commercial television and/or a color monitor. The monitor may accept either a composite video signal or separate chroma and luminance/sync signals in addition to an audio signal. This output is very similar to the ouptut of the 8 pin video C64 units.

The C128 also provides 80 column video interfacing. The available 80 column display is RGBI and monochrome, able to interface to most RGBI TYPE I monitors and most 80 column compatible monochrome monitors.

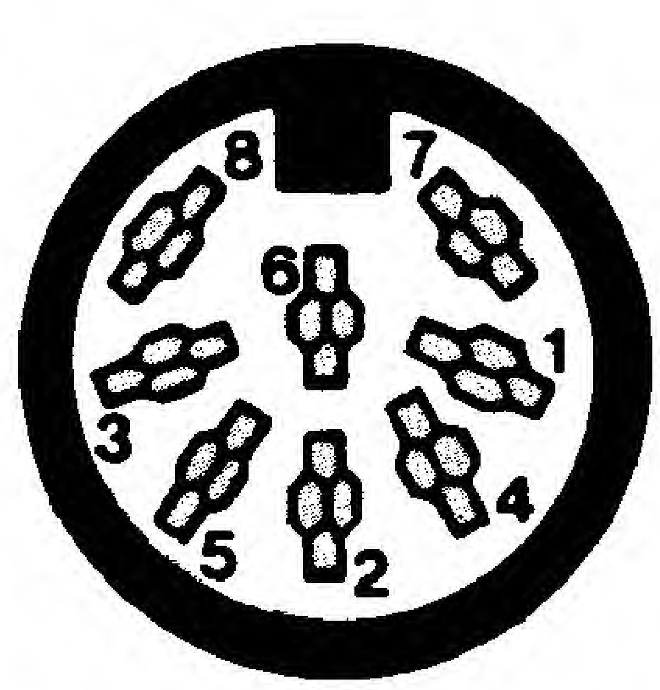
The VIC Video Interface

The VIC video interface supplies a 40 column display in sixteen colors. The VIC signal is available at RF levels at the RF modulator output and at analog levels at the 8 pin DIN monitor connector.

RF Modulator

The modulator provides a broadcast type RF signal carrying the VIC composite video and audio signals. The NTSC modulator is switchable between channels 3 and 4 to help minimize local broadcast interference. The signal generated by the RF modulator complies with FCC ruling concerning FCC Class B, TV interface devices. The RF output is accessible via a standard RCA type phone/video jack.

Monitor Output



CN8

Pin	Signal	Description
1	LUM/SYNC	Luminance/SYNC Ouput
2	GND	
3	AUDIO OUT	
4	VIDEO OUT	Composite signal output
5	AUDIO IN	
6	COLOR OUT	Chroma signal output
7	NC	No connection
8	NC	No connection

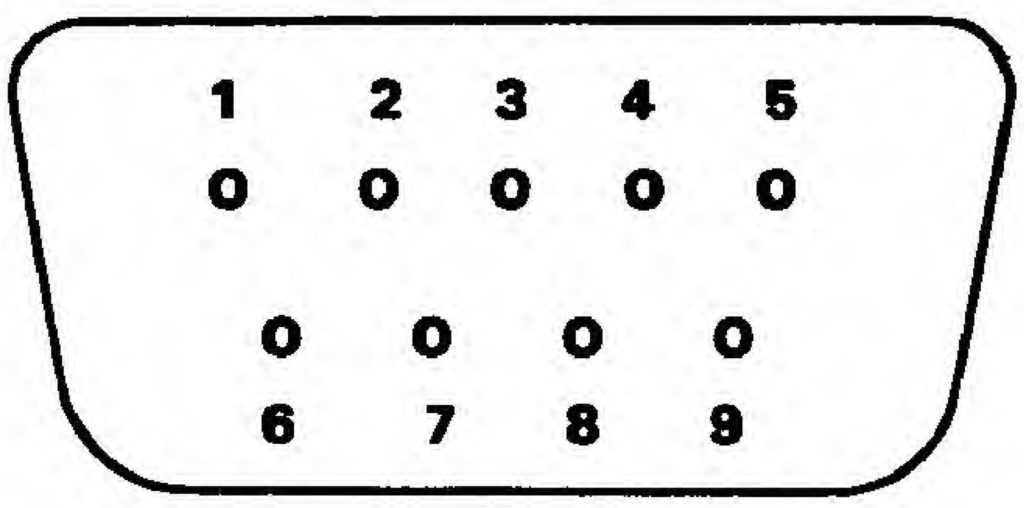
The VIC video output provides the following signals:

Signal	Level	Impedance	DC Offset
Luminance/Sync	1 V p-p	75 Ω	0.5 V
Chroma	1 V p-p	75 Ω	0.5 V
Composite	1 V p-p	75 Ω	0.5 V
Audio	1 V p-p	1K	

The RGBI Video Interface

The 8563 video interface signal, for 80 column display in sixteen colors, is available at digital levels for RGBI and at a three-level derived analog for black and white composite video.

Monitor Output



CN10

Pin	Signal
1	Ground
2	Ground
3	Red
4	Green
5	Blue
6	Intensity
7	Monochrome
8	Horizontal Sync
9	Vertical Sync

The 8563 output provides the following signals:

Signal	Level	Impedance
Red	TTL	TTL
Green	TTL	TTL
Blue	TTL	TTL
Intensity	TTL	TTL
HSync	TTL	TTL
VSync	TTL	TTL
Composite		75Ω
Full Intensity	2.0V	
Half Intensity	1.5V	
Sync	0.5V	

THE 8564 VIDEO INTERFACE CHIP

FOLD OUT SCHEMATIC SHEET 3, PAGE 75, FOR EASY REFERENCE.

The 8564 VIC chip used in the C128 is an updated version of the VIC chip used in current C64 systems. It contains all of the video capabilities of the earlier 6567 VIC chip, including high resolution bit mapped graphics and movable image blocks. It also supports new features used by the C128 system, including extended keyboard scanning. Its register map is upward compatible with the old VIC, allowing compatibility in C64 mode. It is powered by a single 5V DC source, instead of the two sources required by the old VIC chip.

Summary of functions that remain the same as the 6567 VIC:

- Standard Color Character Display Mode
- Multicolor Character Display Mode
- Extended Color Character Display Mode
- Standard Bit Map Mode
- Multicolor Bit Map Mode
- Movable Image Blocks
- Movable Image Block Magnification
- Movable Image Block Priority
- Movable Image Block Collision Detection
- Screen Blanking
- Row/Column Display Select
- Smooth Scrolling
- Light Pen
- Raster Compare Interrupt

As these functions exist in the previous VIC, their description is purposely kept to a minimum. The new functions, however, are described in detail below. Additional Functions of 8564 VIC:

Extended Keyboard Scanning

The 8564 contains a register called the **Keyboard Control Register.** This register allows scanning of three additional keyboard control lines on the C128 keyboard. Thus, the C128 keyboard can have advanced additional keys in C128 mode, while still retaining complete C64 keyboard compatibility in C64 mode. In this register, register 47, bits 0-2 are directly reflected in output lines K_0 to K_2, while bits 3-7 are unused, returning high when read.

2 MHz Operation

The VIC chip contains a register which allows the C128 system to operate at 2 MHz instead of the standard 1 MHz of the C64. This operating speed, however, disallows the use of the VIC chip as a display processor. This bit is bit zero in register 48, and setting this bit enables 2 MHz mode. During 2 MHz operation, the VIC is disabled as a video processor. The μProcessor spends the cycle full time on the bus, while VIC is responsible only for dynamic RAM refresh and DMA arbitration. Clearing this bit will bring back 1 MHz operation and allow the use of the VIC as a video display chip. During refresh and I/O access, the system clock is forced to 1 MHz regardless of the setting of this bit.

Bit one of this register contains a chip testing facility. For normal operation this bit must be clear. None of the other bits in this register are connected.

System Clock Control

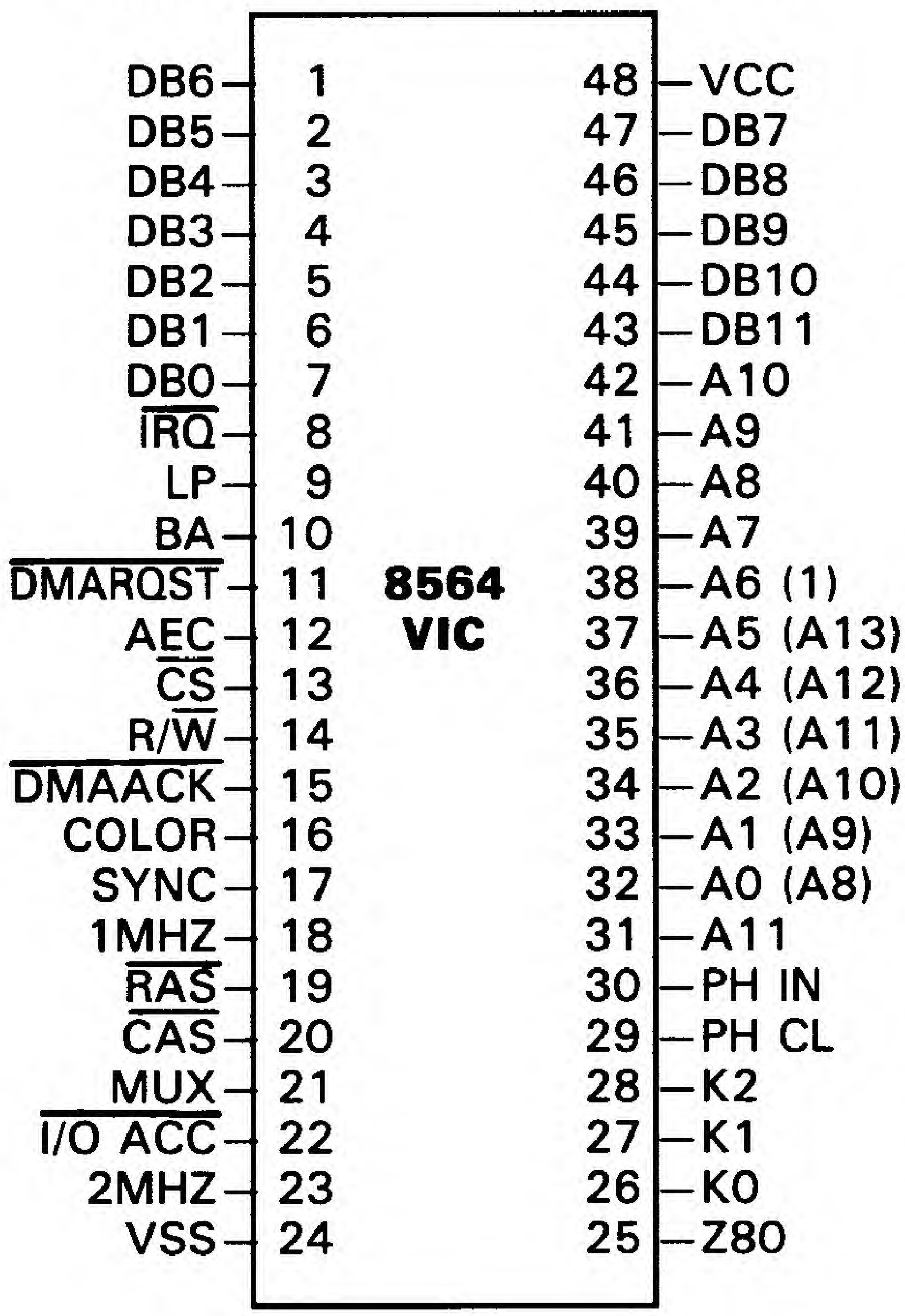
The new VIC chip generates several clocks used by the C128 system. The main clock is the 1 MHz clock, which operates at approximately 1 MHz at all times. Most bus operations and all I/O operations take place in reference to this clock. The next clock to consider is the 2 MHz clock. This clock clocks selected system components, such as the processor, at 2 MHz when in 2 MHz mode. The VIC chip monitors the $\overline{\text{IOACC}}$ input, which indicates the access of an I/O chip, and when asserted, will stretch the 2 MHz clock to synchronize all 2 MHz parts with the 1 MHz I/O parts. Finally, the last clock is the Z-80 clock, which is a 4 MHz clock that only takes place during the low half of the 1 MHz clock. One final note is that since I/O parts look only at the 1 MHz clock, all I/O timings remain the same no matter what the 2 MHz clock is doing.

DMA and Bus Arbitration

True DMA of the internal processor can now be accomplished by requesting the DMA through VIC. The VIC will shut down the processor in an orderly fashion, instead of a suicidal fashion. A DMA source requests a DMA via the DMARQST input. VIC will respond to that request with a DMAACK after shutting down the processor. The DMA source must listen to the DMAACK line and be prepared to itself be shut down in the event that VIC decides to do its own DMA. Thus, the VIC chip has the highest DMA priority. The C128 system does not use this DMA arbitration scheme, but a fatal DMA scheme similar to that of the C64.

THE 8564 VIDEO INTERFACE CHIP (Continued)

315009
8564 VIDEO INTERFACE CHIP

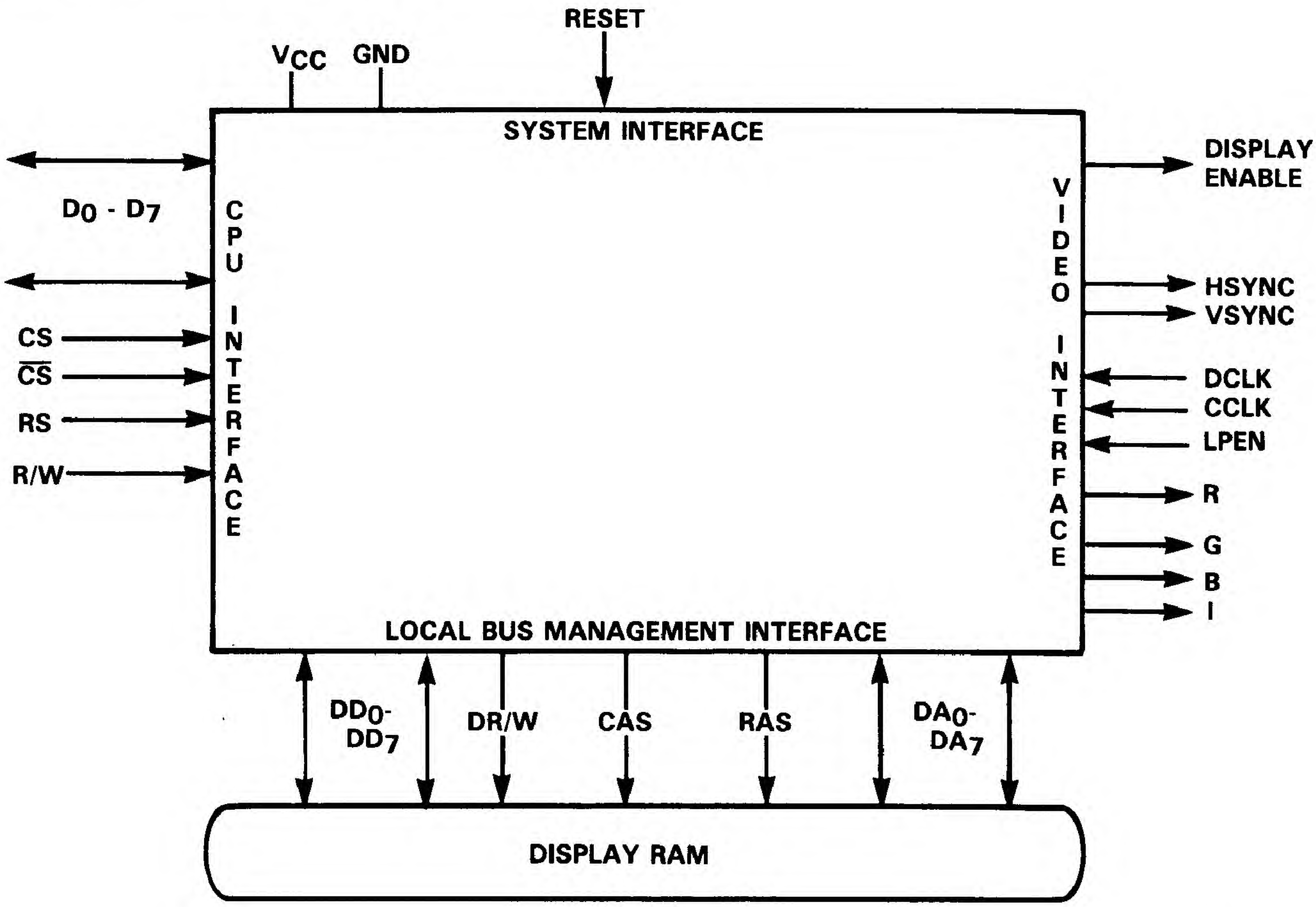


1-7,47	DB0-DB7	These are the bidirectional Data Bus signals. They are for communication between the VIC and the processor, and can only be accessed during AEC high.
8	IRQ	Interrupt output. Generates a low interrupt signal.
9	LP	Light Pen. Edge triggered latch for light pen input.
10	BA	Bus Available output. Used to DMA the processor.
11	DMARQST	External DMA request input. Pulled high on the C128.
12	AEC	Address Enable Control output. Goes high for processor enable on the shared bus, low for VIC cycle and VIC or external DMA.
13	CS	Chip select input. A low signal selects the VIC chip.
14	R/W	Standard 8502 bus Read/Write for interface between the processor and the various VIC registers.
15	DMAACK	External DMA Acknowledge. Not used in the C128 design.
16	COLOR	Output containing all color based video information: chrominance, color reference burst, and color of display data.
17	SYNC	Output containing composite sync information, video data, and luminance information.
18	1MHz	The 1MHz system clock. All system bus activity is referenced to this clock.
19	RAS	Row Address Strobe output for DRAMS.
20	CAS	Column Address Strobe output for DRAMS.
21	MUX	Address Multiplexing control output for DRAMS.
22	I/O ACC	Input from the PLA, indicating an I/O chip access for clock stretching.
23	2MHz	This is the changing system clock, which will be either 1MHz or 2MHz. If the 2MHz bit is clear, no VIC or external DMA is taking place, and no I/O operation is occurring, the clock will be 2MHz. It will be 1MHz otherwise.
24	VSS	Ground.
25	Z80 PHI	The special 4MHz Z-80 clock.
26-28	K0-K2	Extended keyboard strobe bits.
29	PH CL	The Color Clock input, used to derive the chroma signal, 14.31818 MHZ NTSC.
30	PH IN	The fundamental shift rate clock input, also called the DOT clock. Used as the reference for all system clocks. Determines the dot transfer rate to the display.
31	A11	See A8-A11 below.
32-37	A0-A5	Multiplexed Address Lines. During row address time, A_0 - A_5 are driven on A_0 - A_5. During column address time, A_8 - A_{13} are driven on A_0 - A_5 and A_6 is held at one. During a processor write or read, A_0 - A_5 serve as address inputs which latch on the low edge of RAS.
38, 39	A6, A7	Used as VIC address lines.
31, 40-42	A8-A11	Static Address lines. These address lines are used for non-multiplexed VIC memory accesses, such as to Character ROM and Color RAM.
43-46	DB8-DB11	These are the extended data bus signals. They are used for VIC communication with the Color RAM.
47	DB7	See Pins 1-7, 47, DB0-DB7.
48	VCC	5VDC input.

THE 8563 VIDEO CONTROLLER

FOLD OUT SCHEMATIC SHEET 3, PAGE 75, FOR EASY REFERENCE.

The 8563 is a HMOSII technology, custom, 80 column, color video display controller. The 8563 supplies all necessary signals to directly interface to 16K of DRAM, including refresh, and generates RGBI for use with an external RGBI monitor.



There are many different signals involved with the 8563 chip, but they can generally be divided into three categories. The CPU Interface signals serve as an interface to the 8502 bus. The Local Bus Management signals serve to maintain the local memory bus. Finally, the Video Interface signals are those signals that are necessary to provide an RGBI image on an RGBI monitor.

The 8563 chip interfaces directly to the 8502 bus using a minimum of signals. This is due mainly to the local memory used by the 8563.

The Local Bus Management Interface is a group of signals generated by the 8563 for the management of local video DRAM. This local DRAM both simplifies the addition of an 80 column video display to the system and enables it to support an 80 column display without taxing its memory resources.

The final set of 8563 signals are the Video Interface signals. These signals are directly related to the displayed video image.

External Registers

The 8563, which sits at $D600 in the C128, appears to the user as a device consisting of only two registers. These two registers are indirect registers which must be programmed to access the internal set of thirty-seven programming registers. The first register, located at $D600, is called the Address/Status register. When written to, the five least significant bits convey the address of an internal register to be accessed in some way. On a read of this register, a status byte is returned. Bit 7 of this register is low while display memory is being updated, and goes high when ready for the next operation. The 6th bit will return low for a light pen register invalid condition and high for a valid light pen address. The final register indicates with a low that the scan is not in vertical blanking, high that it is in vertical blanking.

The other register is the data register. It can be read and written to. Its purpose is to write data to the internal register selected by the Address register. All internal registers can be read and written to through this register, though not all of them are a full eight bits wide.

Internal Registers

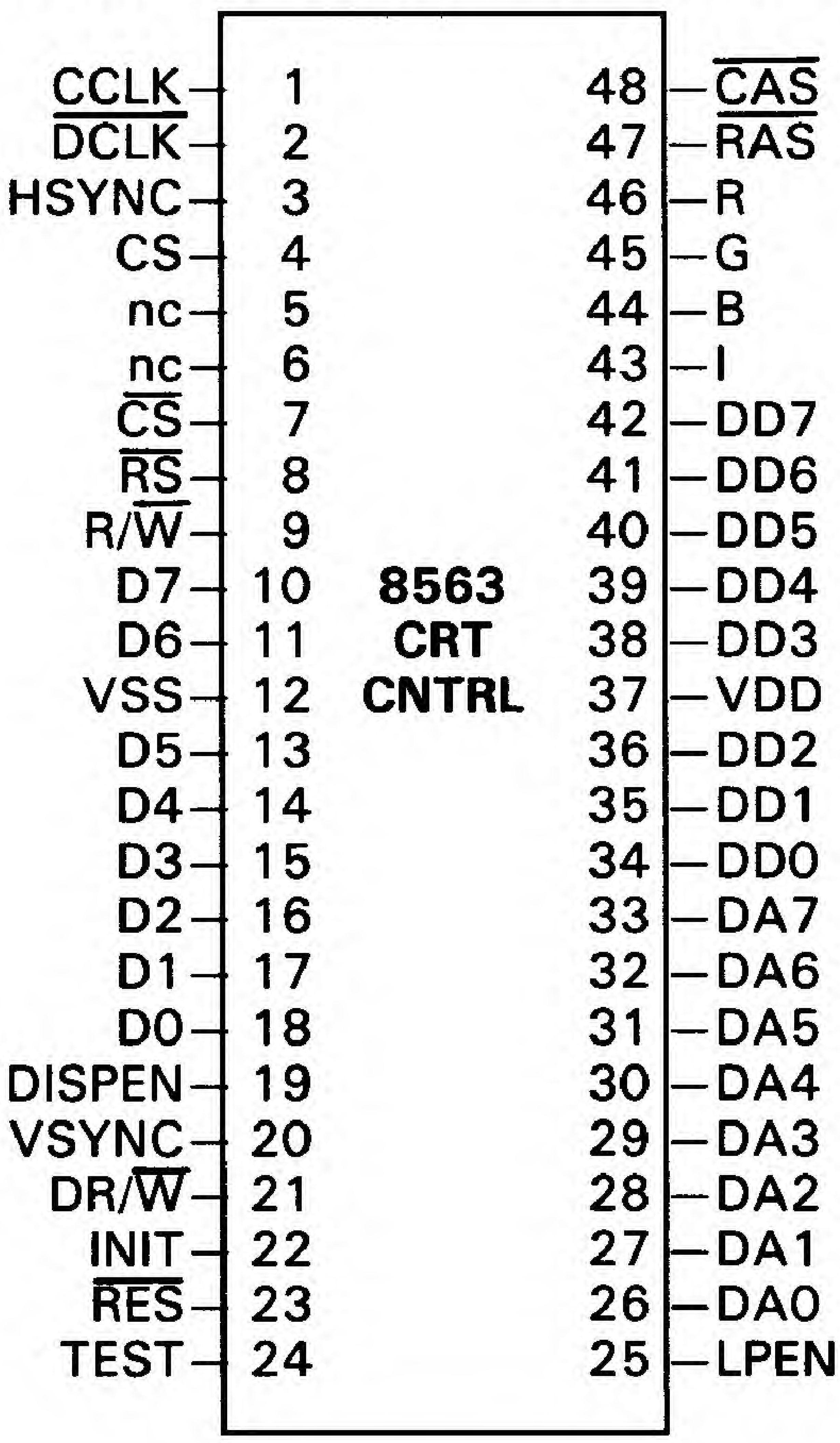
There are thirty-seven internal registers in the 8563, used for a variety of operations. They fall into two basic groups — setup registers and display registers. Setup registers are used to define internal counts for proper video display.

The display registers are used to define and manipulate characters on the screen. Once a character set has been downloaded to the chip, it is possible to display 80 column text in 4-bit digital color. There are also block movement commands that remove the time overhead needed to load large amounts of data to the chip through the two levels of indirection. Below is a display of the 8563 internal register map.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R00	Horizontal Total							
R01	Horizontal Displayed							
R02	Horizontal Sync Position							
R03	Vertical Sync Width				Horizontal Sync Width			
R04	Vertical Total							
R05				Vertical Total Adjust				
R06	Vertical Displayed							
R07	Vertical Sync Position							
R08							Interlace Mode	
R09				Character Total Vertical				
R10		Cursor Mode		Cursor Start Scan Line				
R11				Cursor End Scan Line				
R12	Display Start Address (High)							
R13	Display Start Address (Low)							
R14	Cursor Position (High)							
R15	Cursor Position (Low)							
R16	Light Pen Vertical							
R17	Light Pen Horizontal							
R18	Update Location (High)							
R19	Update Location (Low)							
R20	Attribute Start Address (High)							
R21	Attribute Start Address (Low)							
R22	Character Total-Horizontal				Character Displayed-Horizontal			
R23				Character Displayed-Vertical				
R24	Copy/Fill	Rev Screen	Blink Rate	Vertical Smooth Scroll				
R25	Graph/Text	Atrb Enb	Semigraph	Pix Dbl	Horizontal Smooth Scroll			
R26	Foreground Color				Background Color			
R27	Address Increment per Row							
R28	Character Set Address			4164/4416				
R29				Underline Scan Line				
R30	Word Count (count-1)							
R31	CPU Read/Write Data							
R32	Block Copy Source Address (High)							
R33	Block Copy Source Address (Low)							
R34	Display Enable Begin							
R35	Display Enable End							
R36					DRAM Refresh per Scan Line			

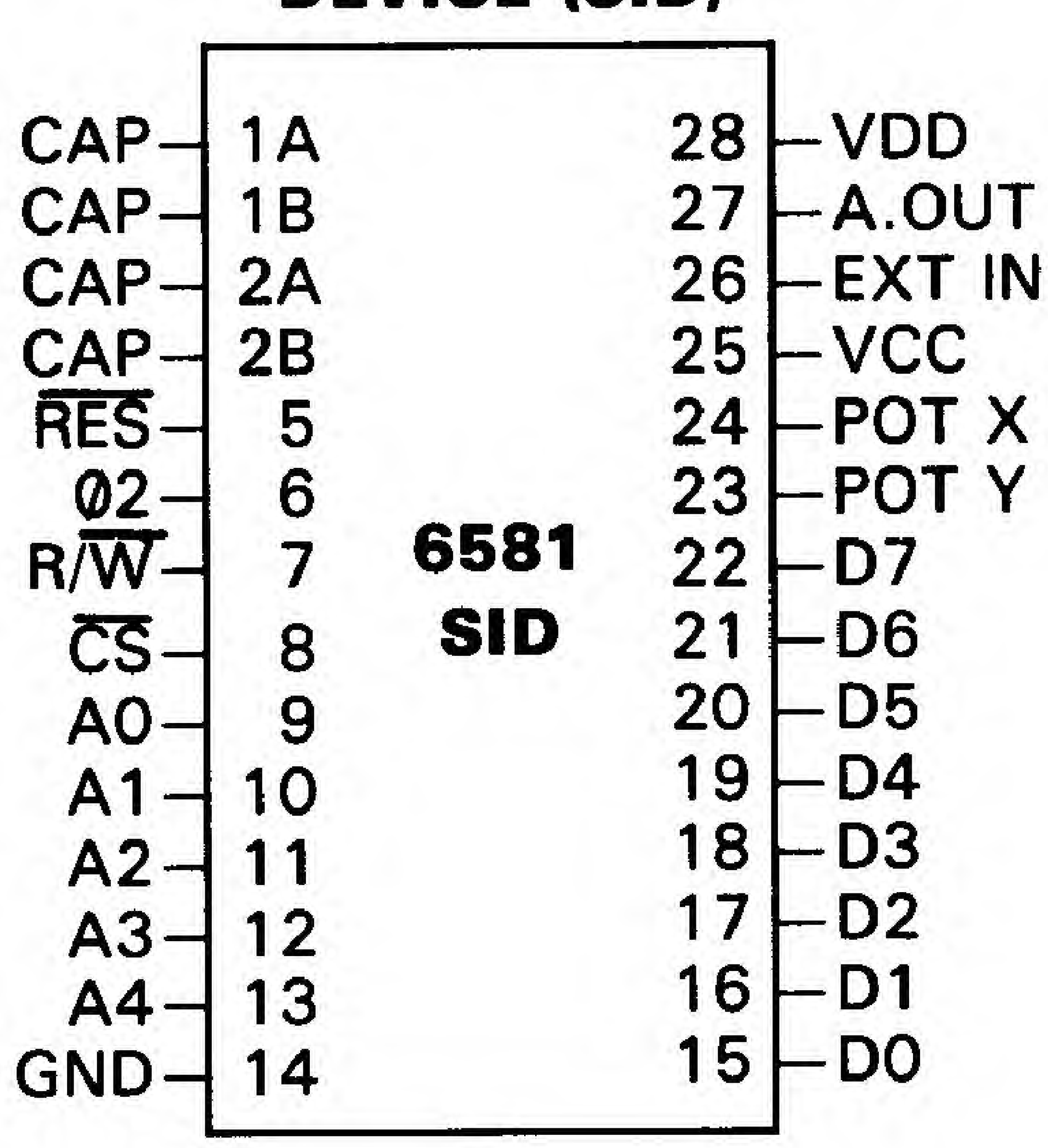
8563 REGISTER MAP

315014
8563 CRT VIDEO CONTROLLER



1	CCLK	Character Clock output.
2	DCLK	Video Dot Clock D.
3	HSYNC	Horizontal Sync Signal.
4	CS	Chip Select input, active high.
5,6	NC	No Connection.
7	CS	Chip Select input, active low.
8	RS	Register Select input. A high allows reads & writes to the selected data register. A low allows reads of the Status register and writes to the Address register.
9	R/W	The read/write line controls the data direction for the data bus. Read is active high, write is active low.
10,11, 13-18	D0-D7	Bi-directional data bus.
12	VSS	Ground.
19	DISPEN	Display Enable output.
20	VSYNC	Vertical Sync signal.
21	DR/W	Local Display DRAM Read/Write.
22	INIT	Active low input for clearing internal control latches.
23	RES	Reset input that initializes all internal scan counters, but not control registers.
24	TEST	Used for testing only — tied to ground.
25	LPEN	Input for Light Pen. A positive going transition on this input latches the vertical and horizontal position of the character being displayed at that time.
26-33,	DA_0-DA_7	Local display DRAM address bus.
34-36, 38-42	DD_0-DD_7	Bidirectional local display DRAM data bus.
37	VCC	5VDC input.
43-46	R,G,B,I	Pixel Data Outputs. A four-bit code is formed, associated with each pixel, containing color/intensity information, allowing a total of 16 colors on grey shades to be displayed.
47	RAS	Row Address Strode for local DRAM.
48	CAS	Column Address Strobe for local DRAM.

906112
6581 SOUND INTERFACE DEVICE (SID)



1,2, 3,4	CAP1A,1B 2A,2B	Capacitor filter connections.
5	RES	Reset input. A low pulse initializes the SID.
6	Ø2	Processor phase 2 clock input.
7	R/W	Processor read/write input.
8	CS	Chip select input.
9-13	A0-A4	Address lines from processor.
14	GND	Dc ground connection.
15-22	D0-D7	Data Bus connections.
23	POT Y	Input to a A/D converter used to detect the value of a variable resistor. Commonly connected to game paddles.
24	POT X	Same as POT Y.
25	VCC	5VDC input.
26	EXT IN	External audio input.
27	Audio out	Audio output, AC coupled to audio amp.
28	VDD	12VDC input.

IC 8568
80 COLUMN CRT CONTROLLER
PN #315092-01

This Circuit implements the features of the 6545E CRT Controller with additional features to increase system integration.

Features

- Single +5 volt power supply.
- Interlaced or non-interlaced display.
- NTSC or PAL operation.
- Shared RAM for Character Data, Pointers and Attributes.
- Cursor and Attributes decoded on-chip.
- R, G, B, I pixel outputs.
- Separate programmable Horizontal and Vertical Sync outputs.
- Character Clock generated on-chip.
- Interfaces to DRAMs with on-chip RAS/CAS timing.
- Programmable character fonts.
- Programmable frame height, width and rate.
- Directly interfaces to 4164 or 4416 DRAMs.

CAS	1	48	RAS
CCLK	2	47	CV
DCLK	3	46	R
HSYNC	4	45	G
CS	5	44	B
CS*	6	43	I
RS	7	42	DD7
R/W	8	41	DD6
INTR	9	40	DD5
D7	10	39	DD4
D6	11	38	DD3
Vss	12	37	Vcc
D5	13	36	DD2
D4	14	35	DD1
D3	15	34	DD0
D2	16	33	DA7
D1	17	32	DA6
D0	18	31	DA5
CSYNC	19	30	DA4
VSYNC	20	29	DA3
DR/W	21	28	DA2
RES	22	27	DA1
INIT	23	26	DA0
TEST	24	25	LPEN

The device is a highly integrated text display chip designed to reduce the parts count of an 80-column display system. The CRT Controller contains the high-speed pixel frequency logic, requiring only a buffer to drive low impedance loads. The CRT Controller is capable of addressing 64K of DRAM memory for Character Data (character fonts), Character Pointers and Attributes. In addition, the DRAM signals RAS, CAS, Read/Write, Data and Multiplexed Addresses are generated on-chip and require no external logic to interface to the DRAMs. The DRAM multiplexed Addresses can be configured via a programmable register bit to interface directly to either 4164 or 4416 Type DRAMs

The device contains an internal 80-column double line buffer. This buffer is loaded with Character Pointers and Attributes during the Horizontal-Blanking interval (and any blank scan lines). These Pointers and Attributes are loaded during one displayed character row for use in the next character row. This device is equivalent to a 2568 or 8568.

The -01 version of the part is intended for use in systems with a TTL level Dclk signal. The -02 version is for systems with a CMOS level Dclk.

PIN DESCRIPTION

CPU INTERFACE

D0-D7	Bidirectional Data Bus interface to the CPU.
CS	Chip Select input (active high).
CS*	Chip Select input (active low).
RS	Register select input. A high allows reads and writes of the selected data register. A low allows reads of the Status Register and writes of the Address Register.
R/W	Read/write input to control D0-D7 data direction. A high allows the CPU to read data supplied by the CRT Controller. A low allows the CRT Controller to accept data written by the CPU.
INTR	Interrupt request output. An open-drain output that is driven low when the Update Ready status bit makes a 'zero' to 'one' transition. This output goes high-impedance when either the Update Ready status bit is a 'zero' or the CPU reads the status register.

VIDEO INTERFACE

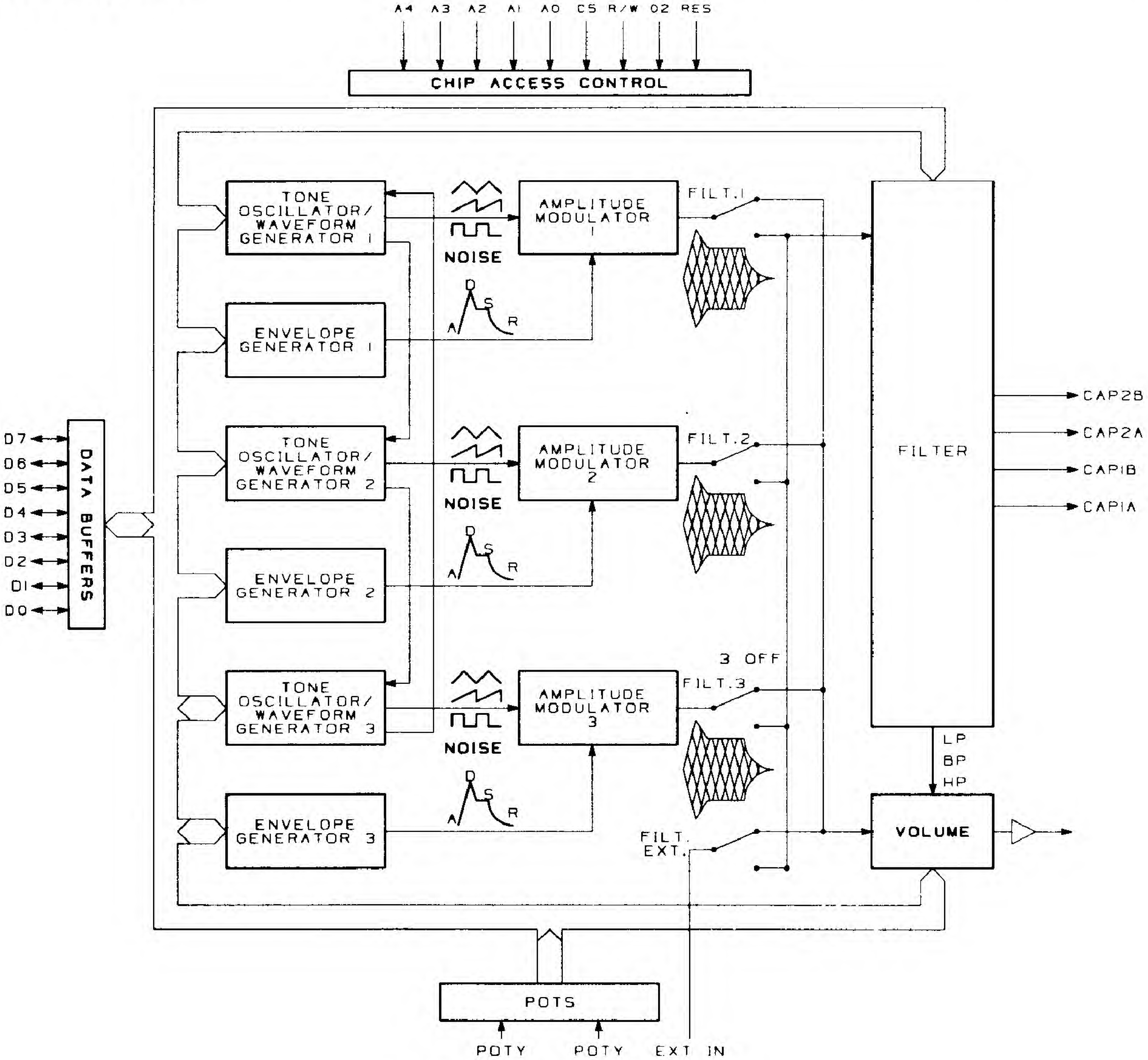
Vcc	5 VDC +/-5%
Vss	0 VDC
RES	Reset input to initalize all internal scan counter circuits. The control registers are not affected. RES can be used to synchronize the display frame to an externally generated signal. This signal should not be confused with the INIT input.
LPEN	Light pen input. A low-to-high transition of the LPEN input loads the internal light pen registers with the vertical and horizontal character poisitions.
DCLK	Dot clock input. Determines the pixel width, DCLK is divided internally to generate the internal character clock and DRAM signals.
HSYNC	Horizontal sync output. HSYNC polarity, position and duration are fully programmable.
VSYNC	Vertical sync output. VSYNC polarity, position and duration are fully programmable.
CSYNC	Composite SYNC output. This is the logical exculsive-nor of internal active-high HSYNC and VSYNC signals.
R, G, B, I	Red, Green, Blue and Intensity outputs. These output a four-bit code associated with each pixel. A total of 16 colors (or shades of gray) may be displayed.
CV	Composite Video output. This is the logical OR of the R, G, and B outputs.
DR/W	Video Display RAM read/write output signal.
DD0-DD7	Video Display RAM bidirectional Data Bus.
DA0-DA7	Video Display RAM multiplexed Address Bus outputs.
RAS	Row Address Strobe output for the multiplexed addresses.
CAS	Column address strobe output for the muliplexed addresses.
CCLK	Character clock output (for unspecified uses).
INIT	Initialization input pin (active low). Clears internal control latches, allowing the CRT Controller to begin proger operation following power-on initialization. The INIT pin should be held low for at least 16 DCLK cycles during system initialization, and held high during operation.
TEST	This pin reconfigures the part to simplify automatic testing. In normal use this pin should be connected to Vss.

8580 SID

Part #318013-01

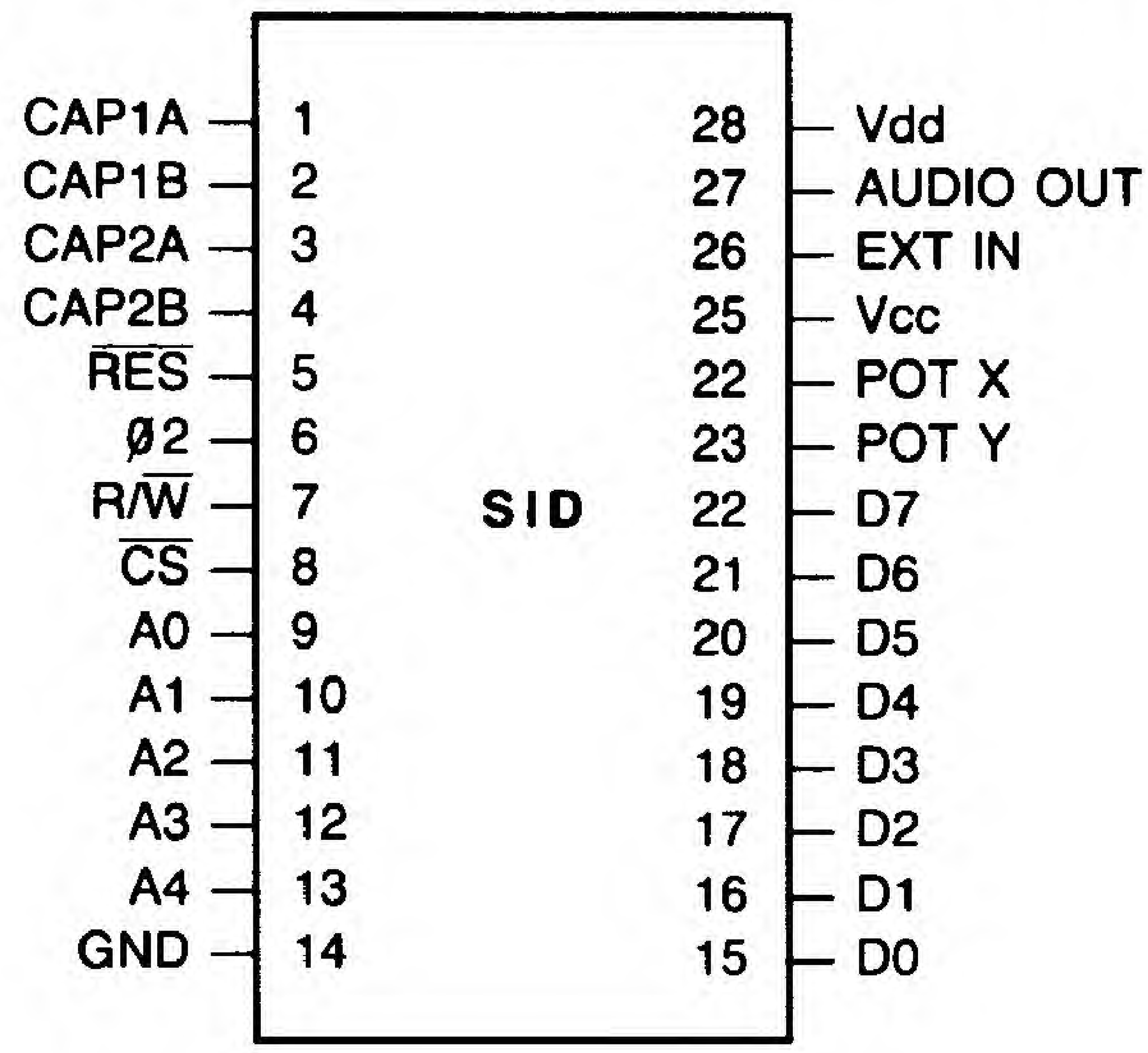
The SID consists of three synthesizer "voices" which can be used independently or in conjunction with each other (or external audio sources) to create complex sounds. Each voice consists of a Tone Oscillator/Waveform Generator, and an Envelope Generator and an Amplitude Modulator. The Tone Oscillator controls the pitch of the voice over a wide range. The Oscillator produces four waveforms at the selected frequency, with the unique harmonic content of each waveform providing simple control of tone color. The volume dynamics of the oscillator are controlled by the Amplitude Modulator under the direction of the Envelope Generator. When triggered, the Envelope Generator creates an amplitude envelope with programmable rates of increasing and decreasing volume. In addition to the three voices, a programmable Filter is provided for generating complex, dynamic tone colors via subtractive synthesis.

SID allows the microprocessor to read the changing output of the third Oscillator and third Envelope Generator. These outputs can be used as a source of modulation information for creating vibrato, frequency/filter sweeps and similar effects. The third oscillator can also act as a random number generator for games. Two A/D converters are provided for inter-facing SID with potentiometers. These can be used for "paddles" in a game environment or as front panel controls in a music synthesizer. SID can process external audio signals, allowing multiple SID chips to be daisy-chained or mixed in complex polyphonic systems.



SID BLOCK DIAGRAM

SID PIN DESCRIPTION



CAPIA, CAPIB (Pins 1,2)/CAP2A, CAP2B (Pins 3,4)

These pins are used to connect the two intergrating capacitors required by the programmable Filter. C1 connects between pins 1 and 2, C2 between pins 3 and 4. Both capacitors should be the same value. Normal operation of the Filter over the audio range (approximately 30Hz-12KHz) is accomplished with a value of 6800 pF for C1 and C2. Polystyrene capacitors are preferred. The frequency range of the Filter can be tailored to specific applications by the choice of capacitor values. For example, a low-cost game may not require full high-frequency response. In this case, larger values for C1 and C2 could be chosen to provide more control over the bass frequencies of the Filter. The approximate maximum Cutoff Frequency of the Filter is given by: FCmax = 8.2E − 5/C
Where C is the capacitor value. The range of the Filter extends approximately 9 octaves below the maximum Cutoff Frequency.

Res (Pin 5)

This TTL-level input is the reset control for SID. When brought low for at least ten 02 cycles, all internal registers are reset to zero and the audio output is silenced. This pin is normally connected to the reset line of the microprocessor or a power-on-clear circuit.

02 (Pin 6)

This TTL-level input is the master clock for SID. All oscillator frequencies and envelope rates are referenced to this clock. 02 also controls data transfers between the SID and the microprocessor. Data can only be transferred when 02 is high. Essentially, 02 acts as a high-active chip select as far as data transfers are concerned. This pin is normally connected to the system clock, with a normal operating frequency of 1.0MHz.

R/W (Pin 7)

This TTL-level input controls the direction of data transfers between SID and the microprocessor. If the chip select conditions have been met, a high on this line allows the microprocessor to Read data from the selected SID register and a low allows the microprocessor to Write data into the selected SID register. This pin is normally connected to the system Read/Write line.

CS (Pin 8)

This TTL-level input is a low active chip select which controls data transfers between SID and the microprocessor CS must be low for any transfer. A Read from the selected SID register can only occur if CS is low, 02 is high and R/W is low. This pin is normally connected to address decoding circuitry, allowing SID to reside in the memory map of a system.

SID PIN DESCRIPTION *(Continued)*

A0-A4 (Pins 9-13)

These TTL-level inputs are used to select one of the 29 SID registers. Although enough addresses are provided to select 1 of 32 registers, the remaining three register locations are not used. A Write to any of these three locations is ignored and a Read returns invalid data. These pins are normally connected to the corresponding address lines of the microprocessor so that SID may be addressed in the same manner as memory.

GND (Pin 14)

For best results, the ground line between SID and the power supply should be separate from the ground lines to other digital noise at the audio output.

D0-D7 (Pins 15-22)

These bidirectional lines are used to transfer data between SID and the microprocessor. They are TTL compatible in the output mode and capable of driving 2 TTL loads in the output mode. The data buffers are usually in the high-impedance off state. During a Write operation, the data buffers remain in the off (input) state and the microprocessor supplies data to SID over these lines. During a Read operation, the data buffers turn on and SID supplies data to the microprocessor over these lines. The pins are normally connected to the corresponding data lines of the microprocessor.

POTX, POTY (Pins 24, 23)

These pins are inputs to the A/D converters used to digitize the position of potentiometers. The conversion process is based on the time constant of a capacitor tied from the POT pin to ground, charged by a potentiometer tied from the POT pin to +5 volts. The component values are determined by:
RC = 1.04E-3
Where R is the maximum resistance of the pot and C is the capacitor. The larger the capacitor, the smaller the POT value jitter. The recommended values for R and C are 470K Ohms and 2200 pF. Note that a spearate pot and cap are required for each POT pin.

Vcc (Pin 25)

As with the GND line, separate +5 VDC line should be run between SID Vcc and the power supply in order to minimize noise. A bypass capacitor should be located close to the pin.

Ext In (Pin 26)

This analog input allows external audio signals to be mixed with the audio output of SID or processed through the Filter. Typical courses include voice, guitar and organ. The input impedence of this pin is in the order of 100K Ohms. External input amplitude should not exceed 3 volts p-p.
Due to the DC level at the external input pin, external signals should be AC-coupled to EXT IN by an electrolytic capacitor in capacitor in the 1-10μF range. As the direct audio path (FILTEX = 0) has unity gain, EXT IN can be used to mix outputs of many SID chips by daisy-chaining. The number of chips that can be chained in this manner is determned by the amount of noise and distortion allowable at the final output. Note that the output Volume control will affect not only the three SID voices, but also any external inputs.

Audio Out (Pin 27)

This open-source buffer is the final audio output of SID, composed of the three SID voices, the Filter and any external input. The output level is set by the output Volume control and reaches a maximum of approximately 3 volts p-p at a 4.75 VDC level.
The output of SID rides on a 4.75 level, it should be AC-coupled to any audio amplifier with an electrolytic capacitor in the 1-10μF range.

Vdd (Pin 28)

As with Vcc, a separate +9 VDC line should be run to SID Vdd and a bypass capacitor should be used.

EQUAL-TEMPERED MUSICAL SCALE VALUES

The following table lists the numerical values which must be stored in the SID Oscillator frequency control registers to produce the notes of the equal-tempered musical scale. The equal-tempered scale consists of an octave containing 12 semitones (notes): C, D, E, F, G, A, B and C*, D*, F*, G*, A*. The frequency of each semitone is exactly the 12th root of 2 ($\sqrt[12]{2}$) times the frequency of the previous semitone. The table is based on a 02 = clock of 1.0 MHz. Refer to the equation given in the Register Description for use of other master clock frequencies. The scale selected is concert pitch, in which A4-440 Hz. Transpositions of this scale and scales other than the equal-tempered scale are also possible.

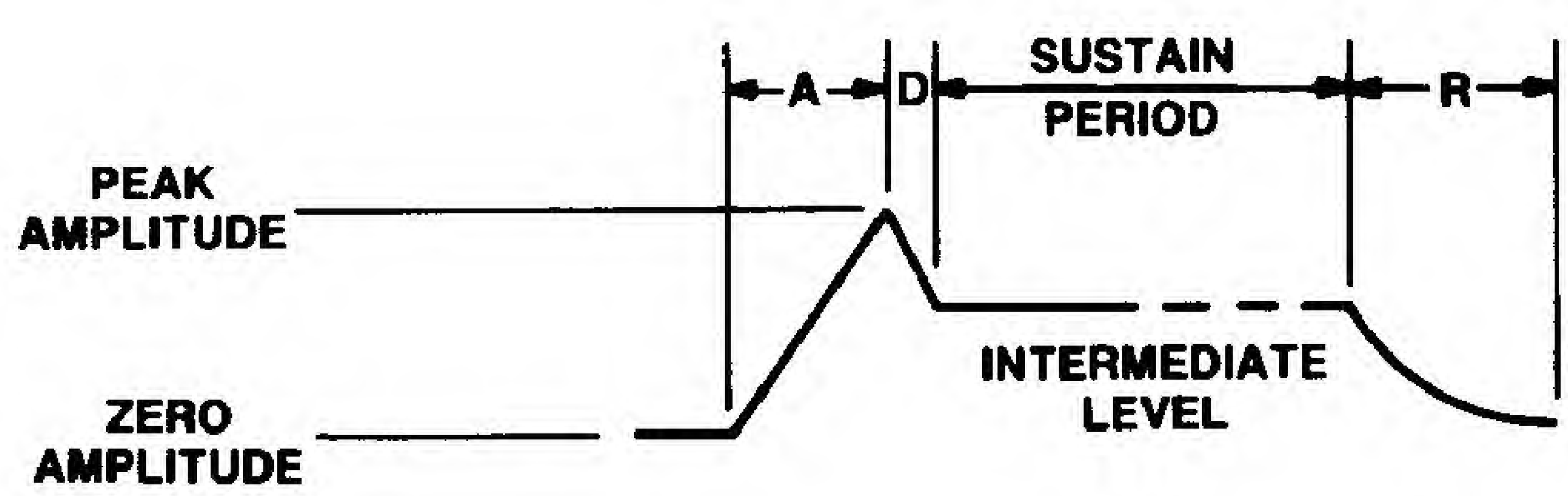
Musical Note	Freq. (Hz)	Osc. Fn. (Decimal)	Osc. Fn. (Hex)	Musical Note	Freq. (Hz)	Osc. Fn. (Decimal)	Osc. Fn. (Hex)
0 C0	16.35	274	0112	48 C4	261.63	4389	1125
1 C0$	17.32	291	0123	49 C4$	277.18	4650	122A
2 D0	18.35	308	0134	50 D4	293.66	4927	133F
3 D0$	19.44	326	0146	51 D4$	311.13	5220	1464
4 E0	20.60	346	015A	52 E4	329.63	5530	159A
5 F0	21.83	366	016E	53 F4	349.23	5859	16E3
6 F0$	23.12	388	0184	54 F4$	370.00	6207	183F
7 G0	24.50	411	018B	55 G4	392.00	6577	1981
8 G0$	25.96	435	01B3	56 G4$	415.30	6968	1B38
9 A0	27.50	461	01CD	57 A4	440.00	7382	1CD6
10 A0$	29.14	489	01E9	58 A4$	466.16	7821	1E80
11 B0	30.87	518	0206	59 B4	493.88	8286	205E
12 C1	32.70	549	0225	60 C5	523.25	8779	224B
13 C1$	34.65	581	0245	61 C5$	554.37	9301	2455
14 D1	36.71	616	0268	62 D5	587.33	9854	267E
15 D1$	38.89	652	028C	53 D5$	622.25	10440	28C8
16 E1	41.20	691	02B3	64 E5	659.25	11060	2B34
17 F1	43.65	732	02DC	65 F5	698.46	11718	2DC6
18 F1$	46.25	776	0308	66 F5$	740.00	12415	307F
19 G1	49.00	822	0336	67 G5	783.99	13153	3361
20 G1$	51.91	871	0367	68 G5$	830.61	13935	366F
21 A1	55.00	923	039B	69 A5	880.00	14764	39AC
22 A1$	58.27	978	03D2	70 A5$	932.33	15642	3D1A
23 B1	61.74	1036	040C	71 B5	987.77	16572	40BC
24 C2	65.41	1097	0449	72 C6	1046.50	17557	4495
25 C2$	69.30	1163	048B	73 C6$	1108.73	18601	48A9
26 D2	73.42	1232	04D0	74 D6	1174.66	19709	4CFC
27 D2$	77.78	1305	0519	75 D6$	1244.51	20897	518F
28 E2	82.41	1383	0567	76 E6	1318.51	22121	5669
29 F2	87.31	1465	05B9	77 F6	1396.91	23436	5B8C
30 F2$	92.50	1552	0610	78 F6$	1479.98	24830	60FE
31 G2	98.00	1644	066C	79 G6	1567.98	26306	6602
32 G2$	103.83	1742	06CE	80 G6$	1661.22	27871	6CDF
33 A2	110.00	1845	0735	81 A6	1760.00	29528	7358
34 A2$	116.54	1955	07A3	82 A6$	1864.65	31234	7A34
35 B2	123.47	2071	0817	83 B6	1975.53	33144	8178
36 C3	130.81	2195	0893	84 C7	2093.00	35115	892B
37 C3$	138.59	2325	0915	85 C7$	2217.46	37203	9153
38 D3	146.83	2463	099F	86 D7	2349.32	39415	99F7
39 D3$	155.56	2610	0A32	87 D7$	2489.01	41759	A31F
40 E3	164.81	2765	0ACD	88 E7	2637.02	44242	ACD2
41 F3	174.61	2930	0B72	89 F7	2793.83	46873	B719
42 F3$	185.00	3104	0C20	90 F7$	2959.95	49660	C1FC
43 G3	196.00	3288	0C08	91 G7	3135.96	52613	CO85
44 G3$	207.65	3484	0D9C	92 G7$	3322.44	55741	O98O
45 A3	220.00	3691	0E6B	93 A7	3520.00	59056	E6B0
46 A3$	233.08	3910	0F46	94 A7$	3729.31	62567	F467
47 B3	246.94	4143	102F	95 B7	3951.06	66288	1F2F0

Although the table above provides a simple and quick method for generating the equal-tempered scale, it is very memory inefficient as it requires 192 bytes for the table alone. Memory efficiency can be improved by determining the note value algorithmically. Using the fact that each note in an octave is exactly half the frequency of that note in the next octave, the note look-up table can be reduced from 96 entries to 12 entries, as there are 12 notes per octave. If the 12 entries (24 bytes) consist of the 16-bit values for the eighth octave (C7 through B7), then notes in lower octaves can be derived by choosing the appropriate note in the eighth octave and dividing the 16-bit value by two for each octave of difference. As division by two is nothing more than a right-shift of the value, the calculation can easily be accomplished by a simple software routine. Although note B7 is beyond the range of the Oscillators, this value should still be included in the

table for calculation purposes (the MSB of B7 would require a special soltware case, such as generating this bit in the CARRY before shifting). Each note must be specified in a form which indicates which of the 12 semitones is desired, and which of the eight octaves the semitone is in. Since four bits are necessary to select 1 of 12 semitones and three bits are necessary to select 1 of 8 octaves, the information can fit in one byte, with the lower nybble selecting the semitone (by addressing the look-up table) and the upper nybble being used by the division routine to determine how many times the table value must be right-shifted.

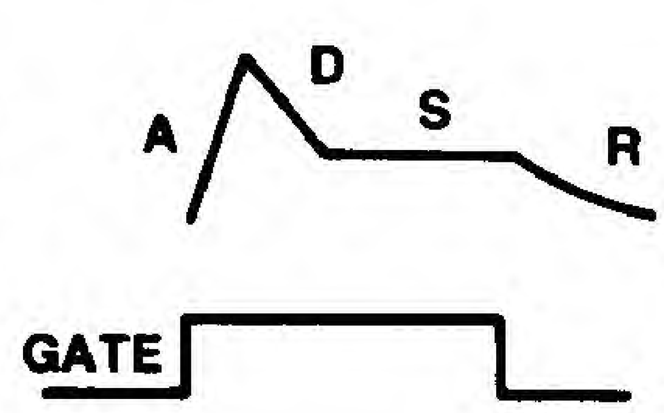
SID ENVELOPE GENERATORS

The four-part ADSR (ATTACK, DECAY, SUSTAIN, RELEASE) envelope generator has been proven in electronic music to provide the optimum trade-off between flexibility and ease of amplitude control. Appropriate selection of envelope parameters allows the simulation of a wide range of percussion and sustained instruments. The violin is a good example of a sustained instrument. The violinist controls the volume by bowing the instrument. Typically, the volume builds slowly, reaches a peak, then drops to an intermediate level. The violinist can maintain this level for as long as desired, then the volume is allowed to slowly die away. A "snapshot" of this envelope is shown below:



This volume envelope can be easily reproduced by the ADSR as shown below, with typical envelope rates:

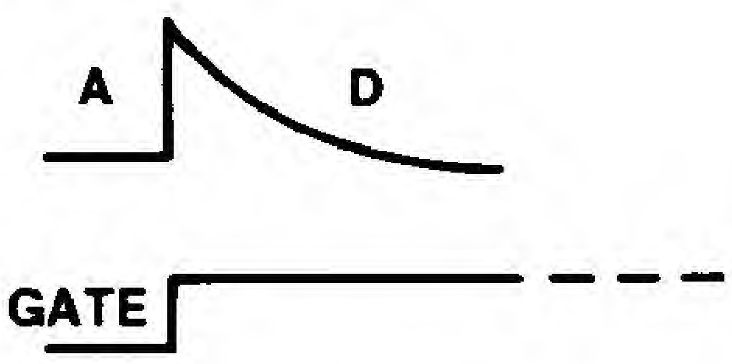
ATTACK:	10 ($A)	500mS
DECAY:	8	300mS
SUSTAIN:	10 ($A)	
RELEASE:	9	750mS



Note that the tone can be held at the intermediate SUSTAIN level for as long as desired. The tone will not begin to die away until GATE is cleared. With minor alterations, this basic envelope can be used for brass and woodwinds as well as strings.

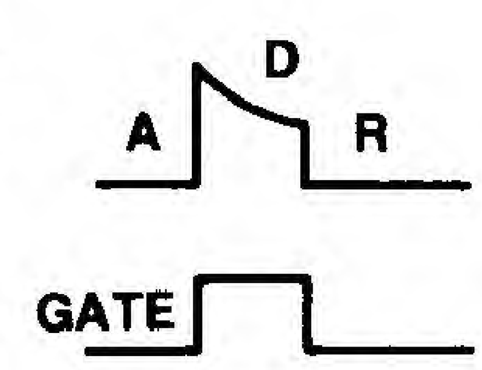
An entirely different form of envelope is produced by percussion instruments such as drums, cymbals and gongs, as well as certain keyboards such as pianos and harpsichords. The percussion envelope is characterized by a nearly instantaneous attack, immediately followed by a decay to zero volume. Percussion instruments cannot be sustained at a constant amplitude. For example, the instant a drum is struck, the sound reaches full volume and decays rapidly regardless of how it was struck. A typical cymbal envelope is shown below:

ATTACK:	0	2mS
DECAY:	9	750mS
SUSTAIN:	0	
RELEASE:	9	750mS



Note that the tone immediately begins to decay to zero amplitude after the peak is reached, regardless of when GATE is cleared. The amplitude envelope of pianos and harpsichords is somewhat more complicated, but can be generated quite easily with the ADSR. These instruments reach full volume when a key is first struck. The amplitude immediately begins to die away slowly as long as the key remains depressed. If the key is released before the sound has fully died away, the amplitude will immediately drop to zero. This envelope is shown below:

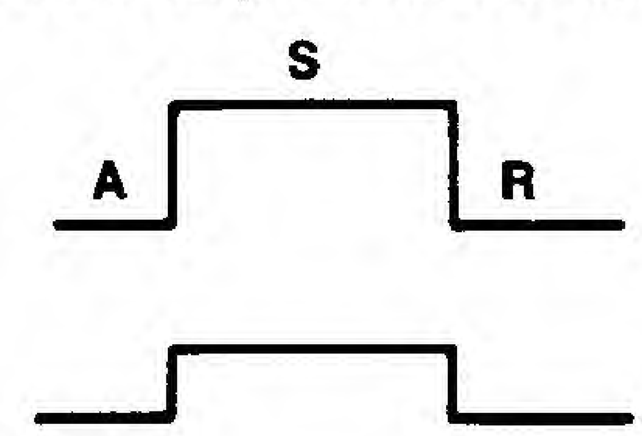
ATTACK:	0	2mS
DECAY:	9	750mS
SUSTAIN:	0	
RELEASE:	0	6mS



Note that the tone decays slowly until GATE is cleared, at which point the amplitude drops rapidly to zero.

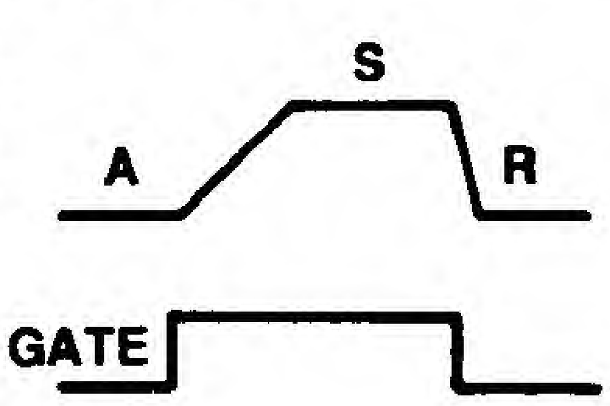
The most simple envelope is that of the organ. When a key is pressed, the tone immediately reaches full volume and remains there. When the key is released, the tone drops immediately to zero volume. This envelope is shown below:

ATTACK: 0	0	2mS
DECAY:	0	6mS
SUSTAIN:	15 ($F)	
RELEASE:	0	6mS

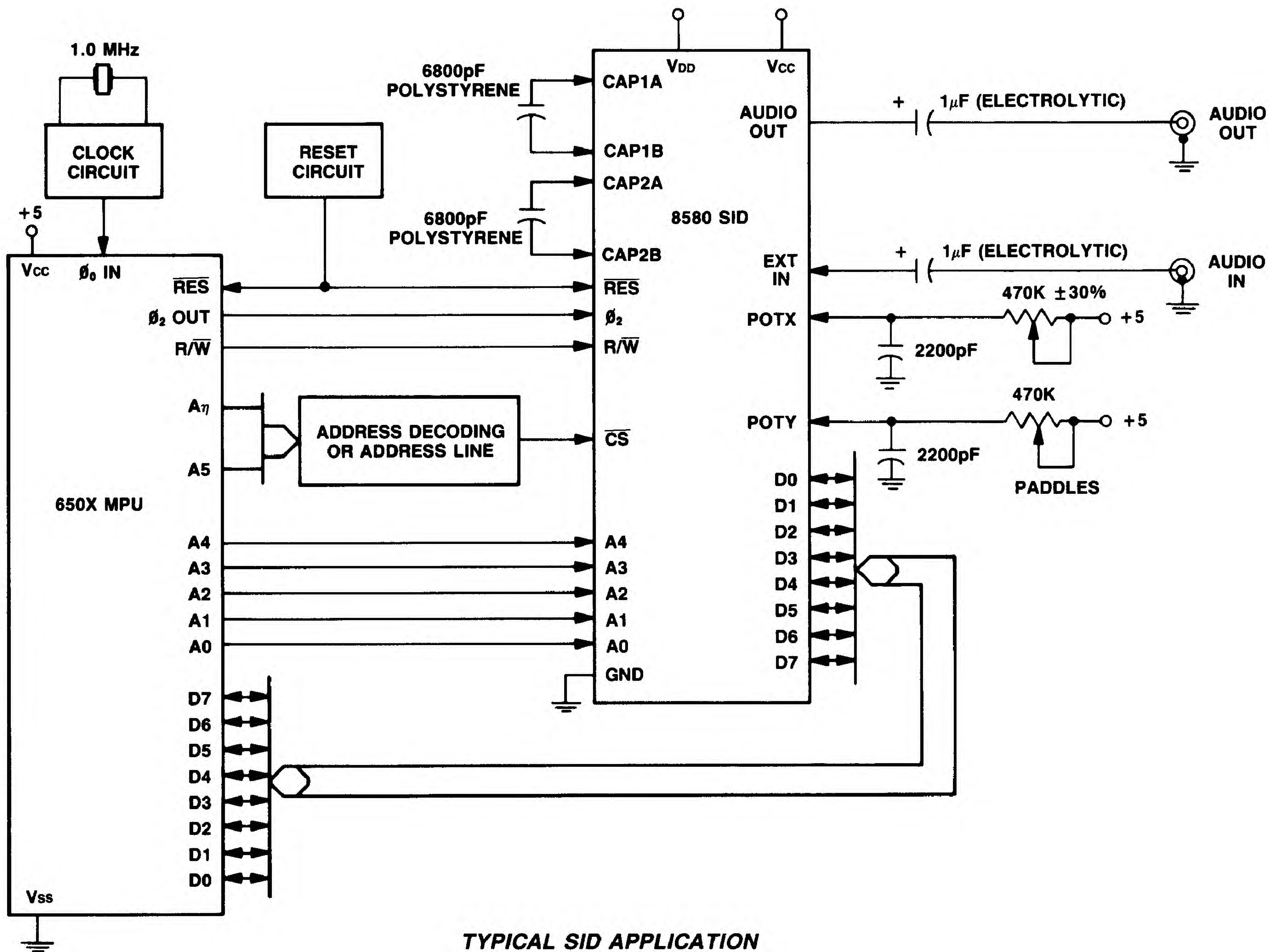


The read power of SID lies in the ability to create original sounds rather than simulations of acoustic instruments. The ADSR is capable of creating envelopes which do not correspond to any "real" instruments. A good example would be the "backwards" envelope. This envelope is characterized by a slow attack and rapid decay which sounds very much like an instrument that has been recorded on tape then played backwards. This envelope is shown below:

ATTACK:	10 ($A)	500mS
DECAY:	0	6mS
SUSTAIN:	15 ($F)	
RELEASE:	3	72mS



Many unique sounds can be created by applying the amplitude envelope of one instrument to the harmonic structure of another. This produces sounds similar to familiar acoustic instruments, yet notably different. In general, sound is quite subjective and experimentation with various envelope rates and harmonic contents will be necessary in order to achieve the desired sound.



TYPICAL SID APPLICATION

FLOPPY DISK DRIVE
READ/WRITE AMPLIFIER
Part #252308-01

FUNCTIONS

This is an integrated circuit designed for Read/Write of Floppy Disk Drive (FDD)

This IC offers the following features:

1. Including Head SW Matrix for selecting Read/Write.
2. The voltage gain of Pre-Amplifier can be selected to 100 or 200 by connecting the external capacitor.
3. Peak Shift is less than 1% over Pre-Amplifier input range of 0.25 mVp-p to 10 mVp-p without adjustment.
4. Time Domain Filter contains retriggerable monostable multivibrator which has internal timing capacitor allowing to be used only external resistor.
5. Common, Write and Erase drivers have large current capacities to satisfy versatile FDD's conditions.
6. Write current can be determined by external resistors and is virtually independent against a change of temperature and power supply voltage.
7. Write current may be selected to two different values by Digital Input signal, if Write current compensation is required on inner tracks of the disk.
8. $\overline{\text{WRITE GATE}}$ and $\overline{\text{ERASE GATE}}$ input timings can be set independently.
9. Power Monitor circuit with Schmitt-Trigger function inhibits illegal writing against power supply voltage fluctuation including power ON/OFF transients.
10. The number of external components is greatly reduced by this one-chip Read/Write IC.

Absolute Maximum Ratings (Ta = 25°C)

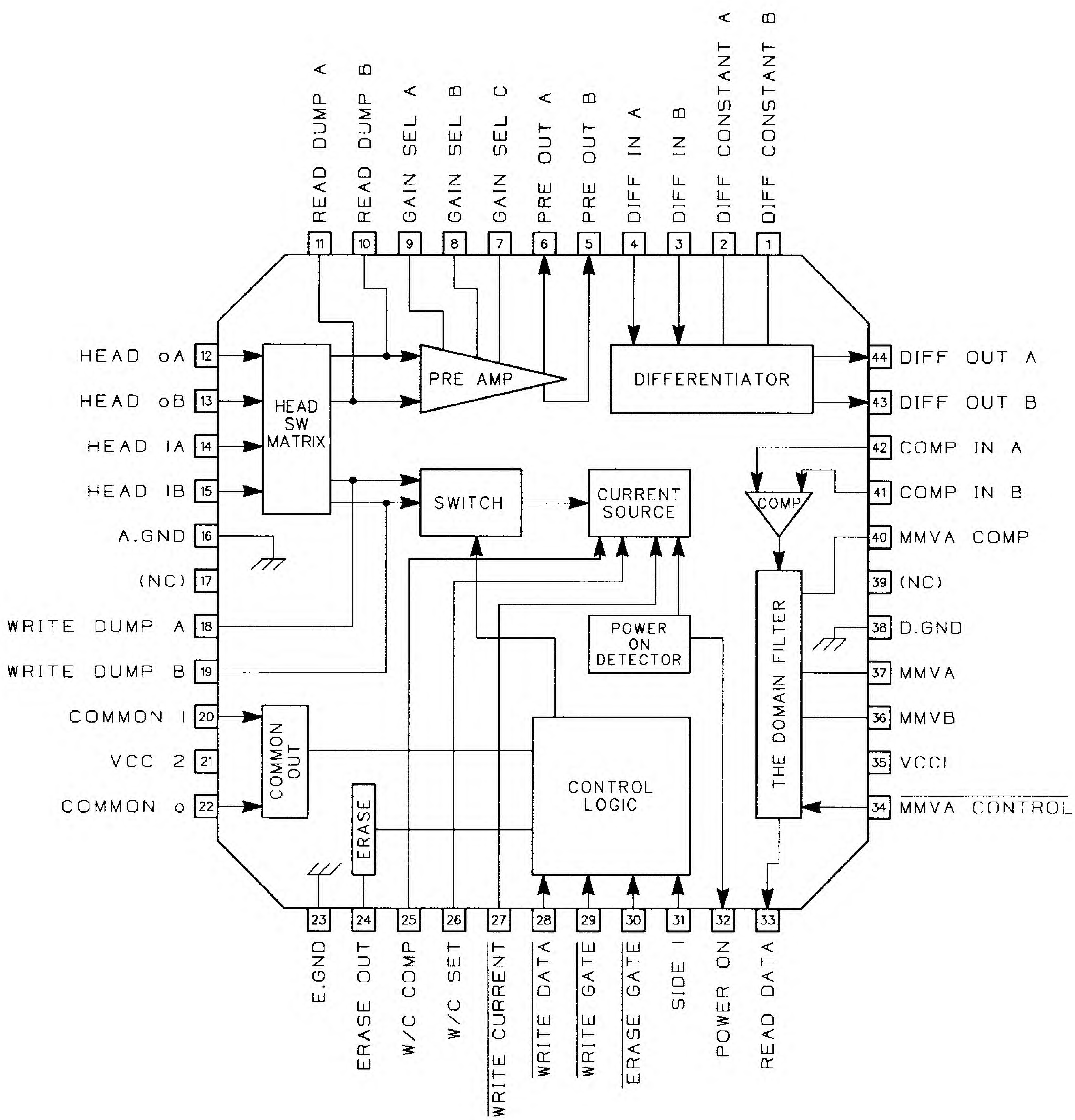
• Power Supply Voltage Vcc:	17V
• Power Supply Voltage Vcc:	7V
• Digital Signal Inputs (NOTE 1) Input Voltage	−0.5 — +5.5V
• POWER ON OUTPUT Voltage Applied	15V
• ERASE OUTPUT Voltage Applied	20V
• COMMON $_0$, COMMON 1, SOURCE Currents	150mA
• POWER ON OUTPUT SINK Current	20mA
• ERASE OUTPUT SINK Current	150mA
• HEAD $_0$A and $_0$B. HEAD 1A and 1B. Voltage Applied	23V
• Operating Ambient Temperature	Topr −20 — +75°C
• Operating Junction Temperature	Tj + 150°C
• Storage Temperature	Tstg −65 — +150°C

NOTE 1: These inputs are $\overline{\text{WRITE CURRENT}}$, $\overline{\text{WRITE DATA}}$, $\overline{\text{WRITE GATE}}$, $\overline{\text{ERASE GATE}}$, $\overline{\text{SIDE 1}}$, and $\overline{\text{MMVA CONTROL}}$.

PIN DESCRIPTION

PIN	DESCRIPTION	FUNCTION
1	DIFF CONSTANT B	Connect external components to set the differential constant.
2	DIFF CONSTANT A	
3	DIFF IN B	Differentiator input
4	DIFF IN A	
5	PRE OUT B	Pre-Amplifier output
6	PRE OUT A	
7,8,9	GAIN SEL A.B.C.	The voltage gain of Pre-Amplifier can be set ot 100 or 200 by connecting a capacitor between these pins.
10	READ DUMP B	Connect the head dumping resistor for Read.
11	READ DUMP A	
12	$HEAD_0$ A	Input and output terminals for Read/Write head on Side $_0$.
13	$HEAD_0$ B	
14	HEAD1 A	Input and output terminals for Read/Write head on Side 1.
15	HEAD1 B	
16	A. GND	Analog circuit Ground.
18	WRITE DUMP A	Connect the head dumping resistor for Write.
19	WRITE DUMP B	
20	COMMON1	Connect the center tap of Read/Write head on Side 1.
21	VCC2	12V Power supply terminal.
22	$COMMON_0$	Connect the center tap of Read/Write head on Side $_0$
23	E. GND	Erase circuit Ground.
24	ERASE OUT	Open Collector Erase current output.
25	W/C COMP	Connect a resistor for Write current compensation.
26	W/C SET	Connect a resistor to determine Write current.
27	$\overline{\text{WRITE CURRENT}}$	Digital input pin. When $\overline{\text{WRITE CURRENT}}$ is set to "L", Write current is increased.
28	$\overline{\text{WRITE DATA}}$	Digtal input pin with Schmitt-Trigged function. When $\overline{\text{WRITE DATA}}$ is set from "H" to "L". Write current is switched.
29	$\overline{\text{WRITE GATE}}$	Digital input pin. When $\overline{\text{WRITE GATE}}$ is set to "L", Write circuit block becomes Active causing Write current to be ON.
30	$\overline{\text{ERASE GATE}}$	Digital input pin. When $\overline{\text{ERASE GATE}}$ is set to "L", Erase circuit becomes Active, causing Erase current to be ON.
31	$\overline{\text{SIDE 1}}$	Digital input pin. When $\overline{\text{SIDE 1}}$ is set to "L", Read/Write head on Side 1 becomes Active.
32	POWER ON	Open Collector output. When Power Monitor circuit detects the power supply voltage drop. POWER ON output is ON.
33	READ DATA	Read Data output (Totem-Pole output).
34	$\overline{\text{MMVA CONT}}$	Digital input pin. When $\overline{\text{MMVA CONT}}$ is set to "L", the pulse width of Time Domain Filter's mono-multi is decreased.
35	VCC1	5V Power supply terminal.
36	MMVS	Connect a resistor to determine the pulse width of Read Data output.
37	MMVA	Connect a resistor to determine the pulse width of Time Domain Filter's mono-multi.
38	D. GND	Digital circuit Ground.
40	MMVA COMP	Connect a resistor for the pulse width compensation of Time Domain Filter's mono-multi.
41	COMP IN B	Comparator input.
42	COMP IN A	
43	DIFF OUT B	Differentiator output.
44	DIFF OUT A	

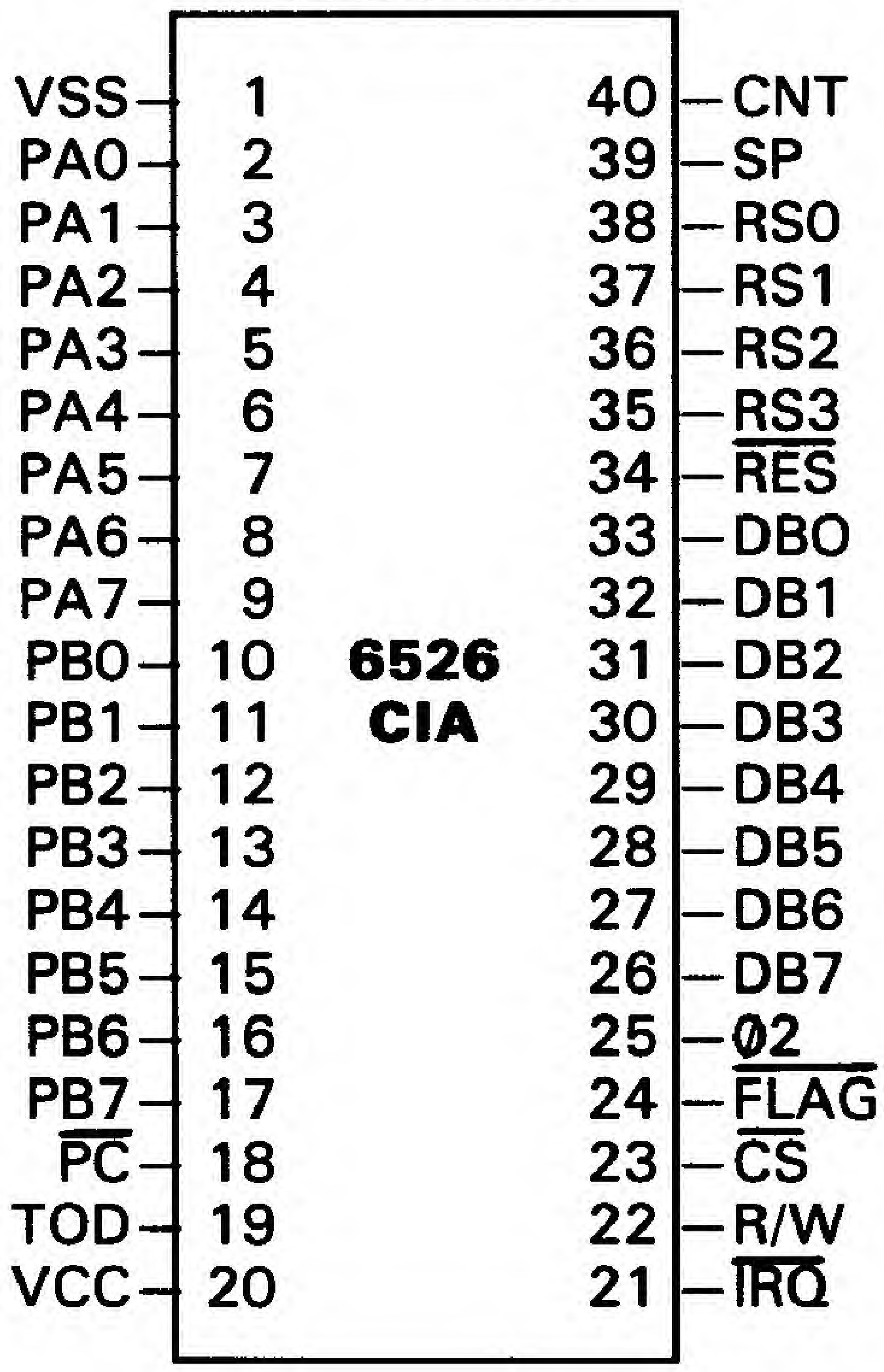
PIN CONFIGURATION



I/O — INPUT/OUTPUT CIRCUITS

FOLD OUT SCHEMATIC SHEET 1, PAGE 73, FOR EASY REFERENCE.

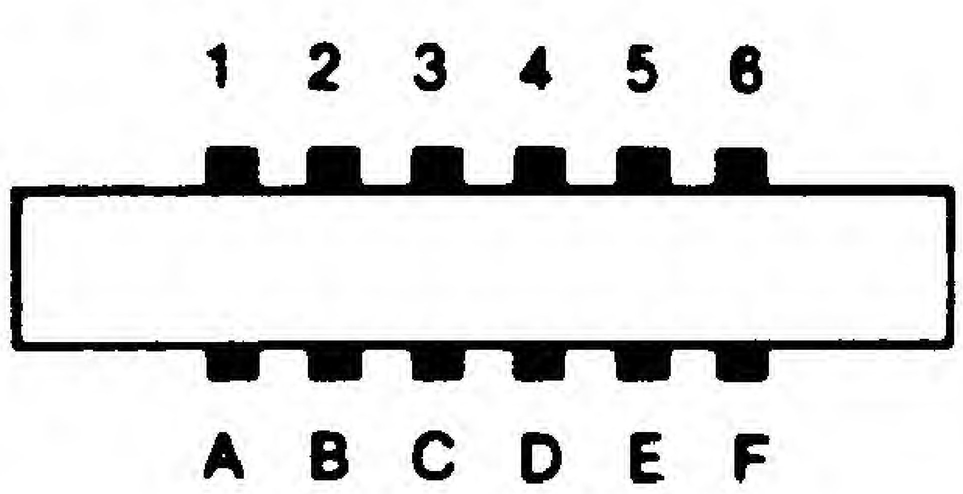
906108
6526 COMPLEX INTERFACE ADAPTER



1	VSS	Ground Connection.
2-9	PA0-PA7	Parallel port A signals. Bidirectional parallel port.
10-17	PB0-PB7	Parallel port B signals. Bidirectional parallel port.
18	PC	Handshake output. A low pulse is generated after a read or write on port B.
19	TOD	Time of day clock input. Programmable 50hz or 60hz input.
20	VCC	5VDC input.
21	IRQ	Interrupt output to microprocessor.
22	R/W	READ/WRITE input from microprocessor's R/W output.
23	CS	Chip select input. A low pulse will activate CIA.
24	FLAG	Negative-edge sensitive interrupt input. Can be used as a handshake line for either parallel port.
25	Ø2	Ø2 clock input.
26-33	DB0-DB7	Bidirectional data bus.
34	RES	Low active reset input. Initializes CIA.
35-38	RS0-RS3	Register select inputs. Used to select all internal registers for communications with the parallel ports, time of day clock, and serial port (SP).
39	SP	Serial Port bidirectional connection. An internal shift register converts microprocessor parallel data into serial data, and visa-versa.
40	CNT	Count input. Internal timers can count pulses applied to this input. Can be used for frequency dependent operations.

CASSETTE INTERFACE

PIN CONFIGURATION

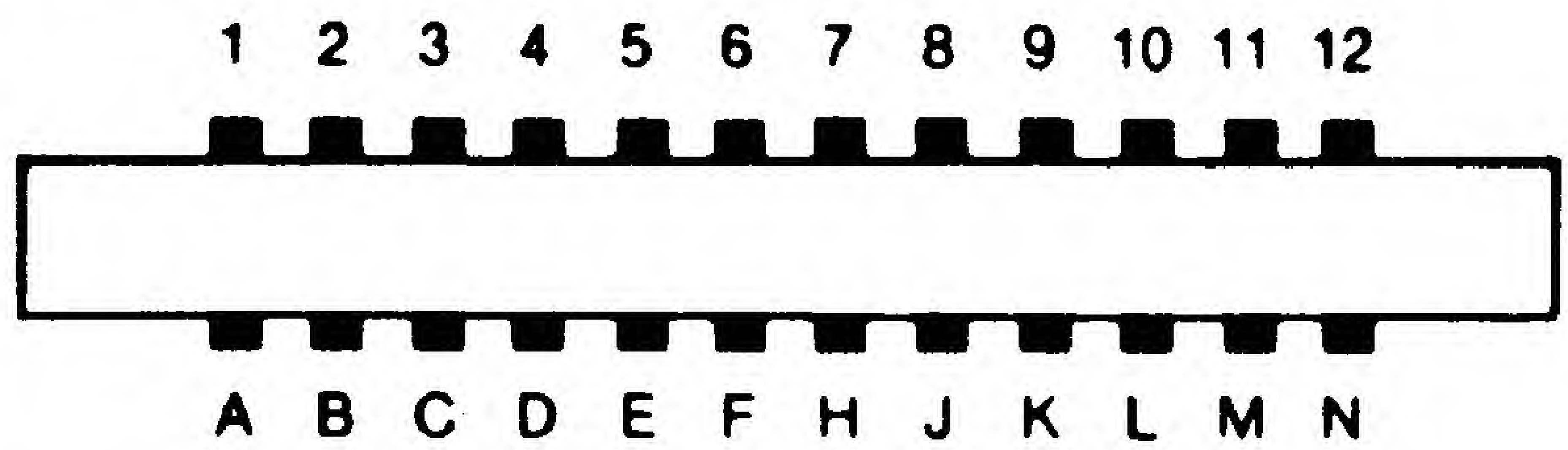


Pin	Signal
A-1	GND
B-2	+5V
C-3	CASSETTE MOTOR
D-4	CASSETTE READ
E-5	CASSETTE WRITE
F-6	CASSETTE SENSE

The Cassette interface is controlled by the 8502 microprocessor. One of the features of the 8502 is a built-in parallel I/O port (P0-P5). P3 - P5 control most of the cassette interface circuitry. P3, pin 27 of U6, outputs the write data signal to connector CN2 on pins E and 5. P4 is an input that senses the play switch depressed on the cassette deck. P5 is an output that controls the cassette motor. When P5 goes "low", pin 12 of the inverter U30 goes "high", Q3 is biased on and current is passed through the cassette motor coil. U1 is a Complex Interface Adapter (CIA). Parallel ports, serial outputs, and Timers are standard features of the CIA. Read data enters on pins D, 4 of CN2. U1 accepts the read data signal on the FLAG input pin 24.

THE USER PORT

PIN CONFIGURATION*

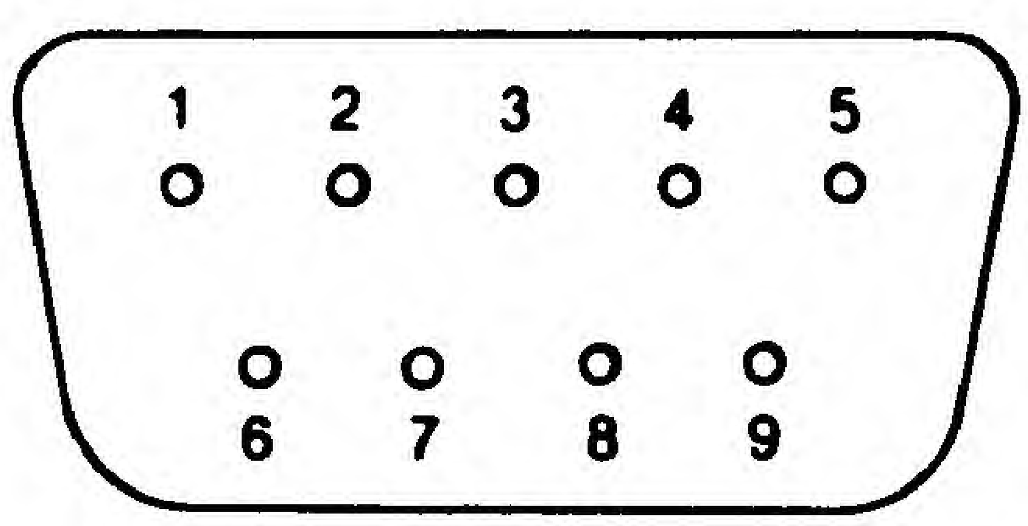


*** See Sheet 1 of Schematic for line definitions.**

Parallel port B of the 6526 CIA device at U4 (PB0-PB7) is made available on the user port. Parallel data transfers with external devices are made very easily through this parallel port. SP1 and SP2 are bi-directional serial ports. CNT1 and CNT2 are bi-directional synchronizing clock signals for each serial port.

THE CONTROL PORTS

PIN CONFIGURATIONS



Control Port 1

Pin	Type	Note
1	JOYA0	
2	JOYA1	
3	JOYA2	
4	JOYA3	
5	POT AY	
6	BUTTON A/LP	
7	+5V	MAX. 50mA
8	GND	
9	POT AX	

Control Port 2

Pin	Type	Note
1	JOYB0	
2	JOYB1	
3	JOYB2	
4	JOYB3	
5	POT BY	
6	BUTTON B	
7	+5V	MAX. 50mA
8	GND	
9	POT BX	

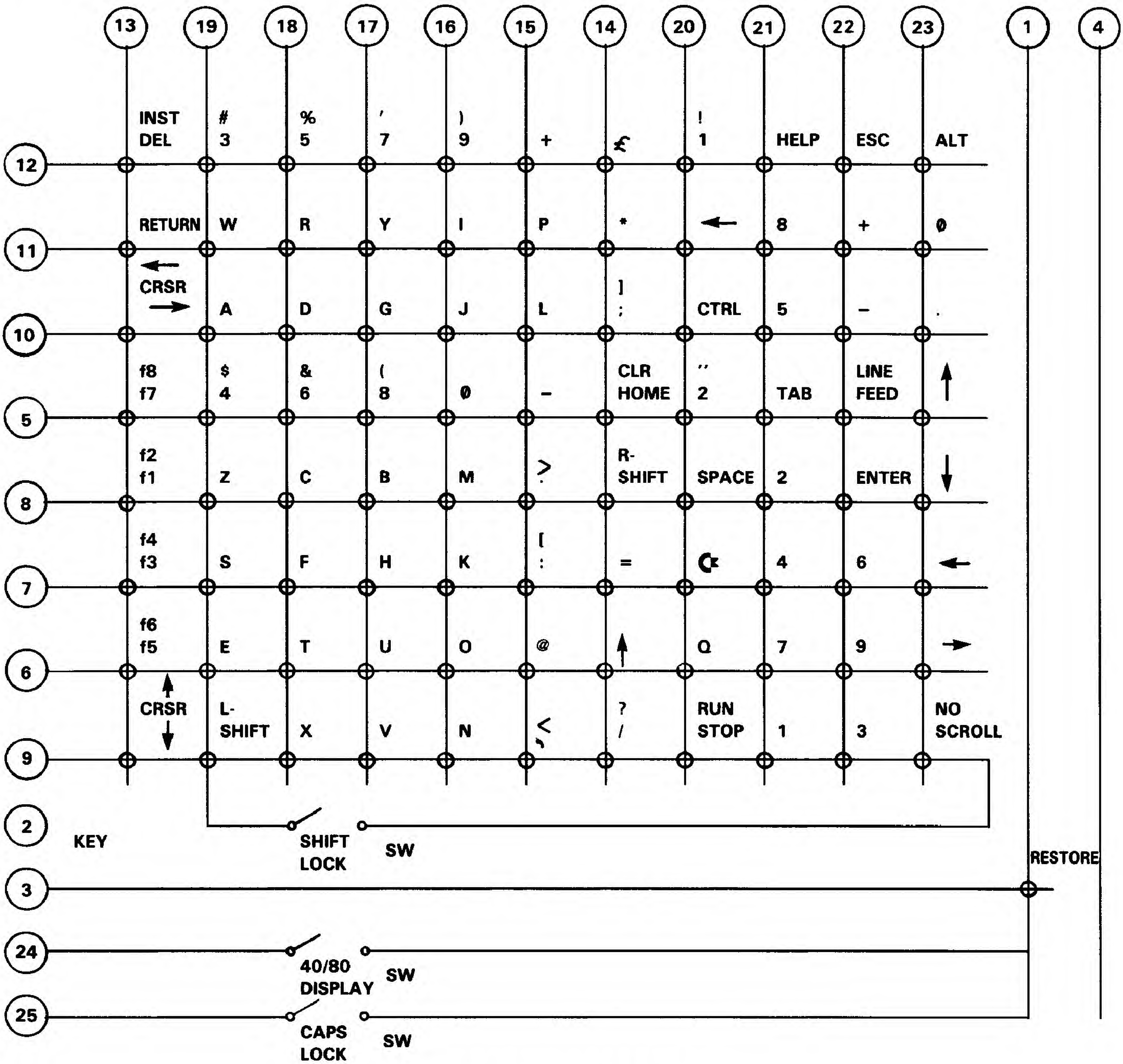
There are two Control ports, numbered 1 and 2. Each Controller port can accept a joystick or game controller paddle. A light pen can be plugged only into port 1, CN3. The control port signals are tied to keyboard inputs and handled by the 6526 CIA device at U1.

THE KEYBOARD

The C128 keyboard is an advance over the standard C64 keyboard. In 64 mode, only the standard 66 keys are accessible.

In 128 mode, 24 extra keys are available. They are the separate CURSOR keys, the HELP key, additional FUNCTION keys, an ALPHA-LOCK key, the 40/80 key and a NUMERIC KEYPAD. These additional keys are strobed by the VIC chip or are tied to dedicated 8502 or MMU I/O lines.

Keyboard operations are controlled by the 6526 I/O device at location U1.

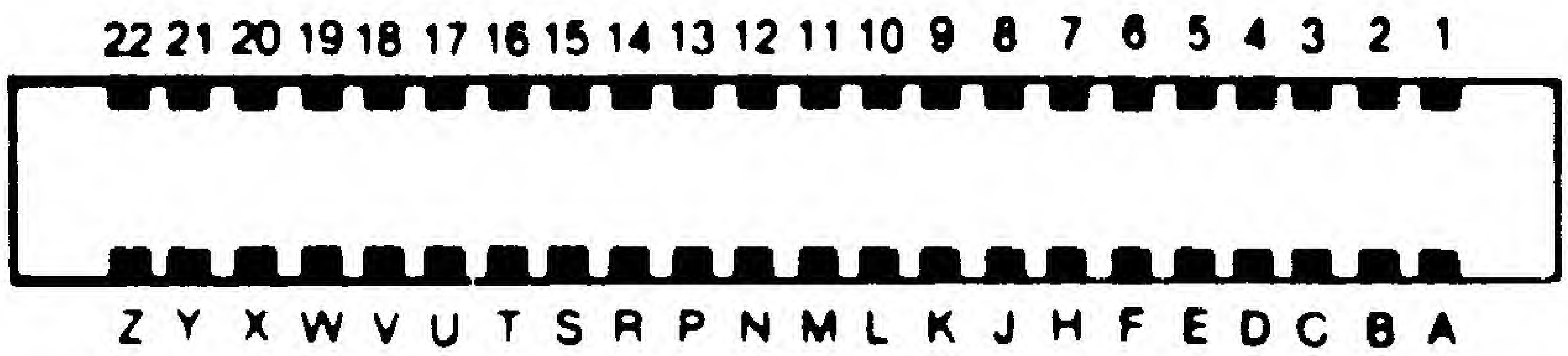


KEYBOARD MATRIX

THE EXPANSION BUS

The expansion bus available at CN1, is a parallel port that is used to connect program or game cartridges as well as special interfaces.

PIN CONFIGURATION*



***See Sheet 1 of Schematic for line definitions.**

The C128 Expansion Bus is compatible with the C64 Expansion Bus, while at the same time allowing extended capabilities in C128 mode.

CARTRIDGE ADDITION

The C128 can use larger and more sophisticated cartridges than the C64 can. One of the main reasons for this is the new banking scheme used in the C128 for external cartridges. The C64 uses two hardware control lines, $\overline{\text{EXROM}}$ and $\overline{\text{GAME}}$, to control banking out of internal facilities and banking in of cartridge facilities. The C128 uses a software polling method, where, upon power-up, it polls the cartridge, according to a defined protocol, to determine if such a cartridge exists, and if so, its software priority. Since the C128 is always free to bank between cartridges and built-in ROM, an external application can take advantage of internal routines and naturally become an extended part of the C128, as opposed to becoming a replacement application.

The elimination of $\overline{\text{EXROM}}$ and $\overline{\text{GAME}}$ as hardware control lines for cartridge identification, in C128 mode, has freed up both of these lines for extended functioning. Both of the lines appear as bits in the MMU mode configuration register, and are both input and output ports. Neither has a dedicated function other than general cartridge function expansion and lend themselves to act as latched banking lines or input sense lines.

DMA Capability

The C128 expansion bus supports DMAs in a fashion similar to that of the C64. A C64 DMA is achieved by pulling the $\overline{\text{DMA}}$ pin on the expansion bus low. Immediately after this happens, the RDY and AEC lines of the processor are brought low. This can cause problems, depending on what the processor is doing at the time. The RDY input of a 65xx series processor, when brought low, will halt the processor on the next ϕ_1 cycle, leaving the processor's address lines reflecting the current address being fetched. However, if the processor is in a write cycle when RDY is brought low, it will ignore RDY until the next read cycle. Thus, in the C64, a $\overline{\text{DMA}}$ input occuring during a write cycle will tri-state the processor's address and data bus, but not stop it until up to three cycles later when the next read cycle occurs. The write cycles following the $\overline{\text{DMA}}$ input do not actually write, causing memory corruption and often processor fatality when the $\overline{\text{DMA}}$ line is released. Any $\overline{\text{DMA}}$ input during ϕ_2 is a potentially fatal DMA.

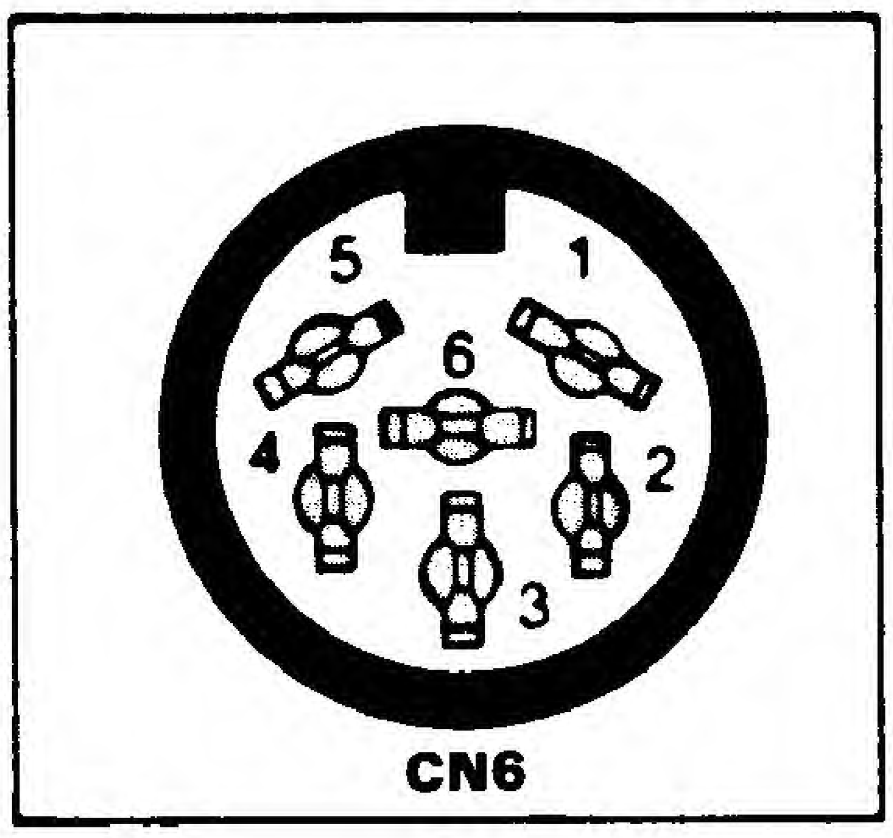
If a proper $\overline{\mathrm{DMA}}$ is asserted, the C64 tri-states and shuts down, allowing the DMA source complete access to the processor bus. Such a DMA source must monitor the ϕ_2 and BA outputs, as it must tri-state when the VIC is on the bus, and it must completely DMA when a VIC DMA is called for. The VIC chip always has the highest DMA priority. When on the bus, the DMA source has access to RAM, ROM, and I/O in the C64 DMA scheme. A proper DMA shutdown is usually achieved via some C64 software handshaking with the DMA source.

The C128 mode uses a similar DMA scheme. When the $\overline{\mathrm{DMA}}$ input goes low, the RDY input to the 8502, the AEC input to the 8502, and the $\overline{\mathrm{BUSRQST}}$ input to the Z-80, immediately go low. Additionally, the gated AEC signal, GAEC, goes low, causing the MMU to go immediately to its VIC cycle mode, and the Z-80 data-out buffer to tri-state. The DMA causes the Address to Shared Address buffer to reverse direction, and the Translated Address to Address buffer to be enabled, giving the external DMA source complete access to the processor Address Bus. The PLA is still looking at ungated AEC and, as such, will allow access to I/O devices, RAM, and ROM. There can be no access to the MMU. Thus, for C128 memory mapping, the memory map must be set up before being DMAed. For C64 mode, memory mapping is done by the 8502 processor port lines and by the external $\overline{\mathrm{EXROM}}$ and $\overline{\mathrm{GAME}}$. Since the 8502 ports will be inaccessible by a DMA source, only C64 map changes based upon $\overline{\mathrm{EXROM}}$ and $\overline{\mathrm{GAME}}$ can be made during a DMA. This is the same as is true in a C64 unit. All DMA sources, as with the C64, must yield to the VIC during ϕ_0 or BA low. In order to use DMAs, the DMA source will most likely have to cooperate with a C128 mode program that allows the C128 to shake hands in software with a DMA source to effect DMA non-destructively. A DMA source may also be able to monitor ϕ_0 and R/W to achieve a non-destructive DMA, since unlike the C64, the C128 does not tri-state the R/W line during VIC time. The R/W line will, of course, tri-state during a DMA to allow the DMA source to drive it, and care must be taken to look at the R/W line for this only after it becomes valid. In any case, ϕ_0 and BA must be constantly monitored to allow the VIC chip to function.

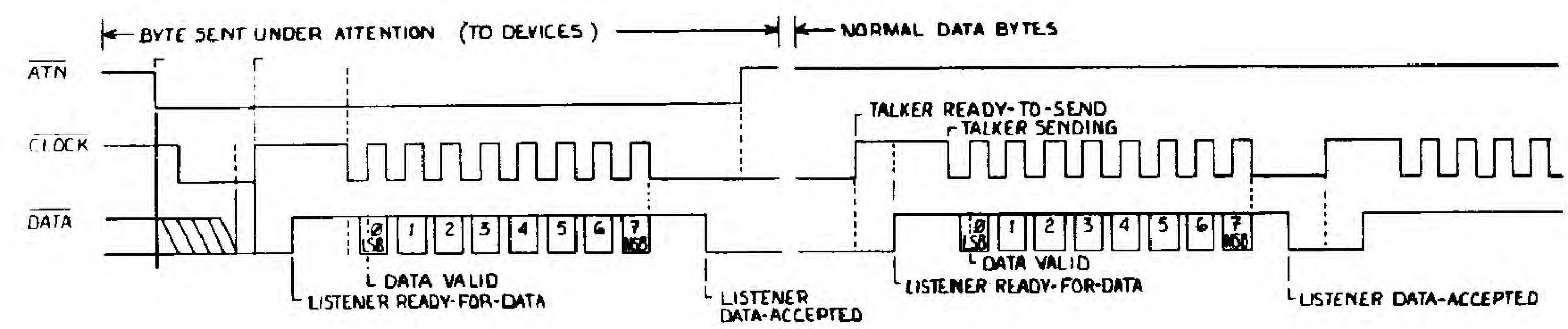
THE SERIAL BUS

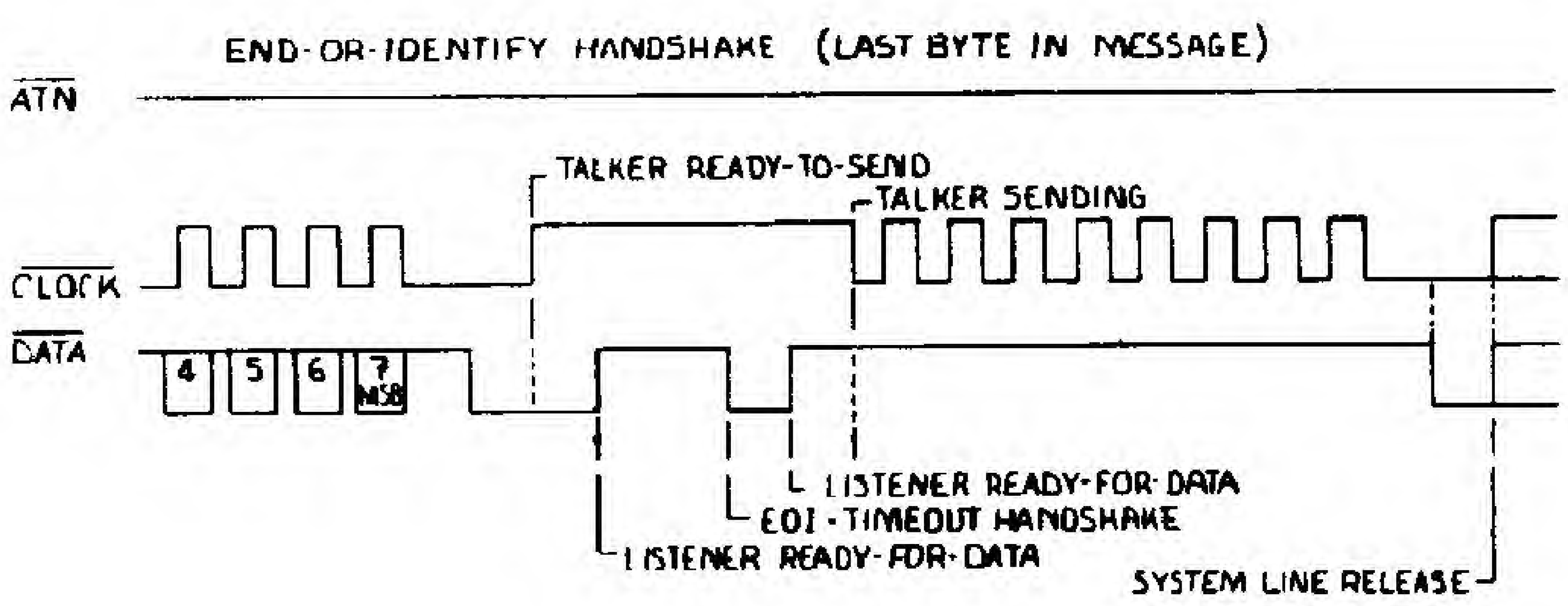
The C128 Serial Bus is an improved version of the C64/VIC 20 serial bus. The C128 improves this bus by allowing communication at much greater speeds with specially designed peripherals, the most important being the disk drive, while still maintaining capability with older, slower peripherals used by the VIC 20 and the C64.

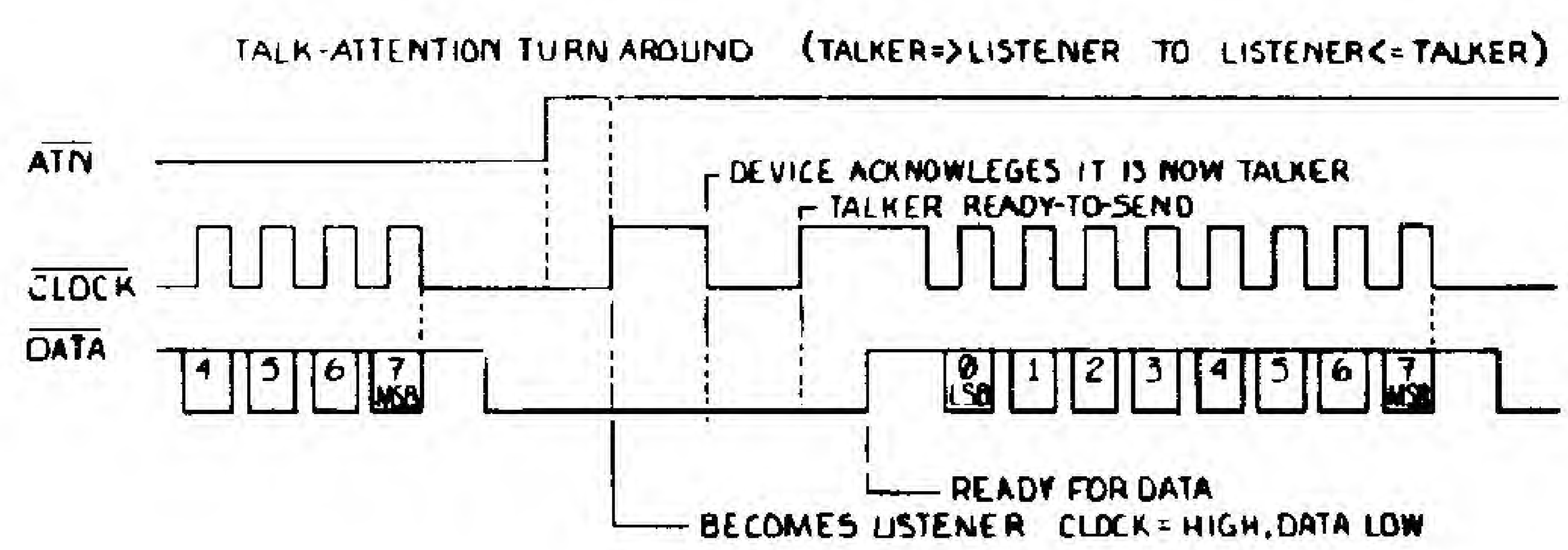
Serial Interface Connector



Pin No.	Signal	Description
1	SERIAL SRQ	The slow serial bus does not use the SERVICE REQUEST line. The fast serial bus uses it as a fast bidirectional clock line.
2	GND	Chassis ground.
3	SERIAL ATN	The ATTENTION line is a low active handshake used to address a device on the bus.
4	SERIAL CLK	This is the slow serial CLOCK. It is used by slow serial devices to clock data transmitted on the serial bus.
5	SERIAL DATA	The bidirectional serial DATA line is used by both slow and fast devices to transmit data in sync with a clock signal.
6	$\overline{\text{RES}}$	The RESET line is used to reset all peripherals when the host resets.







Bus Operations

There are three basic bus operations that take place on the serial bus, in both fast and slow modes. The first of these is called **Control**. The C128 is the **controller** in most circumstances. The **controller** of the bus is always the device that initiates protocol on the bus, requesting peripheral devices to do one of the two other serial operations, either **Talk** or **Listen.**

All serial bus devices can listen. A **Listener** is a device that has been ordered by the **Controller** to receive data. Some devices, such as disk drives, can talk. A **Talker** can send data to the **Controller.** Both hardware and software drive this bus protocol.

The Standard (Slow) Serial Bus

The slow serial bus uses the port lines of the 6526 at U4, C1A 2, to drive ATN, CLK and DATA. The operation is the same as that of the C64 and when in C64 mode, slow to fast interference is automatically removed.

The Fast Serial Bus

In order to talk as a fast talker, the Controller must be addressing a fast device. When addressing any device, the C128 sends a fast byte, toggling the SRQ line eight times, with the ATN line low. If the device is a fast device, it will record the fact that a fast Controller accessed it and respond with a fast acknowledge. If the device is a slow device, no response is delivered and the C128 then assumes it is talking with a slow device. The status of the fast or slow is retained until the device is requested to untalk, unlisten, or if an error or system reset occurs.

The fast serial bus, in order to achieve its speed increase, uses different hardware than that of the slow serial bus. The fast serial method is to use the serial port lines of the 6526 U1, CIA 1, pin 39, to actually transfer the serial data. This increases the transfer rate dramatically.

The $\overline{\text{FSDIR}}$ bidirectional control line signals the MMU at U7, pin 44, that a fast device is present. The MMU then outputs control signals to the data direction buffer hardware for fast serial operation.

COMMON LINE DEFINITIONS

A0-A7	PROCESSOR ADDRESS BUS	LCR	LOAD CONFIGURATION REGISTER
AEC	ADDRESS ENABLE CONTROL	LP	LIGHT PEN INPUT
ATN	ATTENTION LINE		
		MA0-MA11	MULTIPLEXED ADDRESS BUS
BA	BUS AVAILABLE	MMU	MEMORY MANAGEMENT UNIT
		MS 0-4	MEMORY STATUS, ALSO INDENTIFIED AS ROMBANK
C128/64	C128 OR C64 MODE		
CAP LK	CAPITAL LOCK	MUX	ADDRESS MULTIPLEX CONTROL
CAS	DRAM COLUMN ADDRESS STROBE		MEMORY MULTIPLEX
CASENB	RAM COLUMN ADDRESS STROBE ENABLE		
CASS SENSE	CASSETTE SENSE	NMI	NON-MASKABLE INTERRUPT
CASS WRT	CASSETTE WRITE		
CASS MTR	CASSETTE MOTOR	PHI 0	2 MHZ 0 CLOCK
CHAROM	CHARACTER ROM SELECT	POT X,Y	JOYSTICK PORT INPUTS
CIA	COMPLEX INTERFACE ADAPTOR		
CLR BNK	COLOR RAM BANK SELECT	RCR	RAM CONFIGURATION REGISTER
CNT	COUNT INPUT	RESET	SYSTEM RESET
COLORAM	COLOR RAM CHIP SELECT	ROM 1-4	ROM CHIP SELECTS FOR OPERATING SYSTEM
D0-D7	DATA BUS	ROM H,L	CHIP SELECTS FOR EXPANSION ROMS
DA0-DA7	DISPLAY ADDRESS	ROMBANK 0,1	MEMORY STATUS SELECT
DD0-DD7	DISPLAY DATA BUS		
DMA	DIRECT MEMORY ACCESS	RS	REGISTER SELECT
DOT CLK	8.18 MHZ VIDEO DOT CLOCK	RSTR	RESTORE
DRAM	DYNAMIC RAM	R/W	READ/WRITE LINE
DRESET	DYNAMIC RAM RESET		
DWE	DRAM WRITE ENABLE	SA0-SA7	SHARED ADDRESS BUS
EXROM	EXTERNAL ROM ENABLE	TA8-TA15	TRANSLATED ADDRESS BUS
EXTRES	EXTERNAL RESET	TOD	TIME OF DAY
		VA 14,15	VIC ADDRESSES
FROM	FUNCTION ROM	VIC	VERSATILE INTERFACE CHIP
FSDIR	FAST SERIAL DIRECTION	VMA0-VMA7	VIC MULTIPLEXED ADDRESS BUS
GAME	GAME ROM ENABLE	Z80EN	Z-80 ENABLE
GWE	COLOR RAM WRITE ENABLE	Z80 PHI	Z-80 CLOCK
		ZD0-ZD7	Z-80 DATA BUS
I/O	I/O SELECT		
IOACC	I/O ACCESS	1 MHZ	MASTER CLOCK ϕ IN
IRQ	INTERRUPT REQUEST	40/80 SENSE	40/80 COLUMN STATUS SENSE

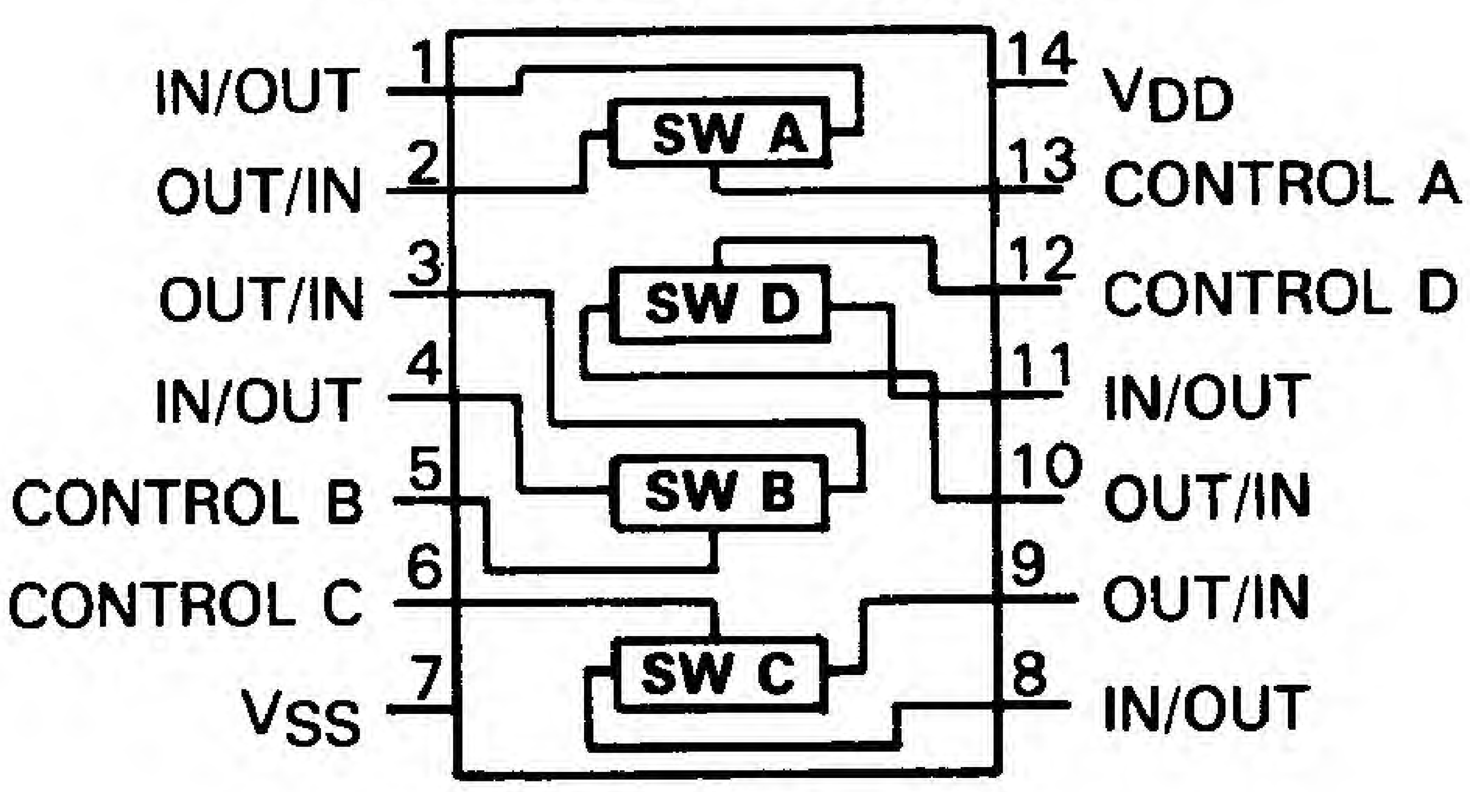
COMMON I.C.'S
PIN ASSIGNMENTS AND LOGIC

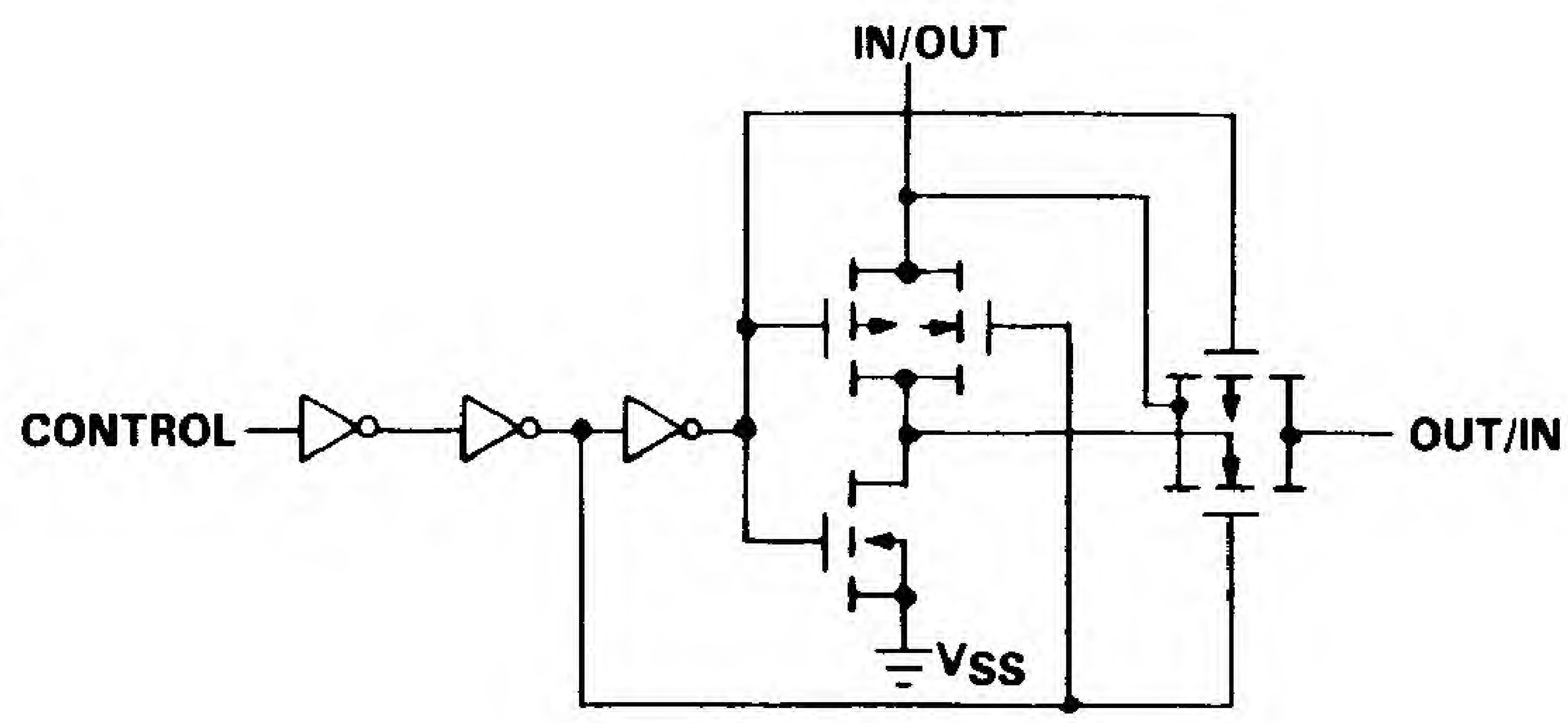
4066
QUAD BILATERAL SWITCH

PIN ASSIGNMENTS

INTERNAL DIAGRAM (EACH SWITCH)

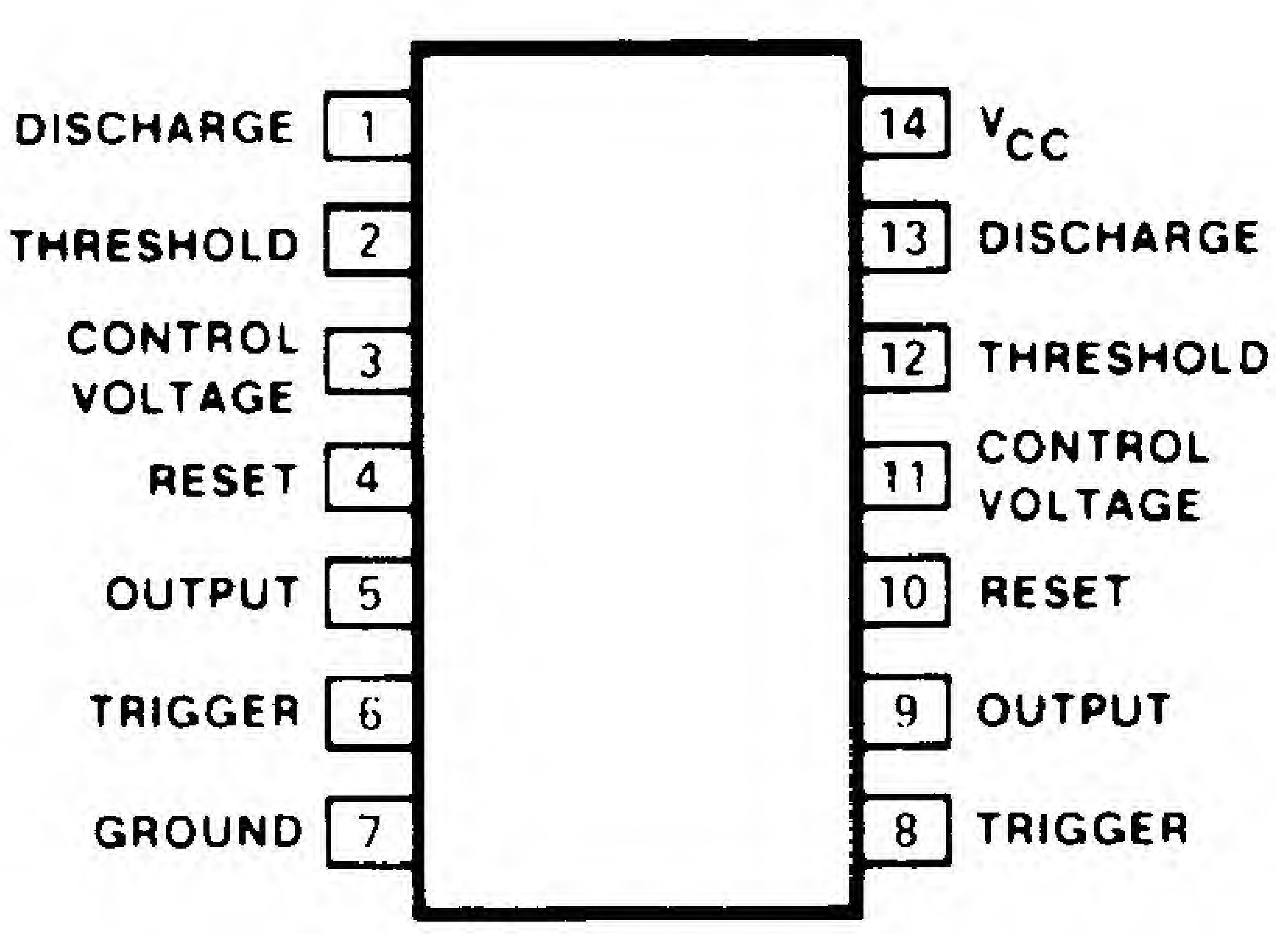
DUAL-IN-LINE PACKAGE

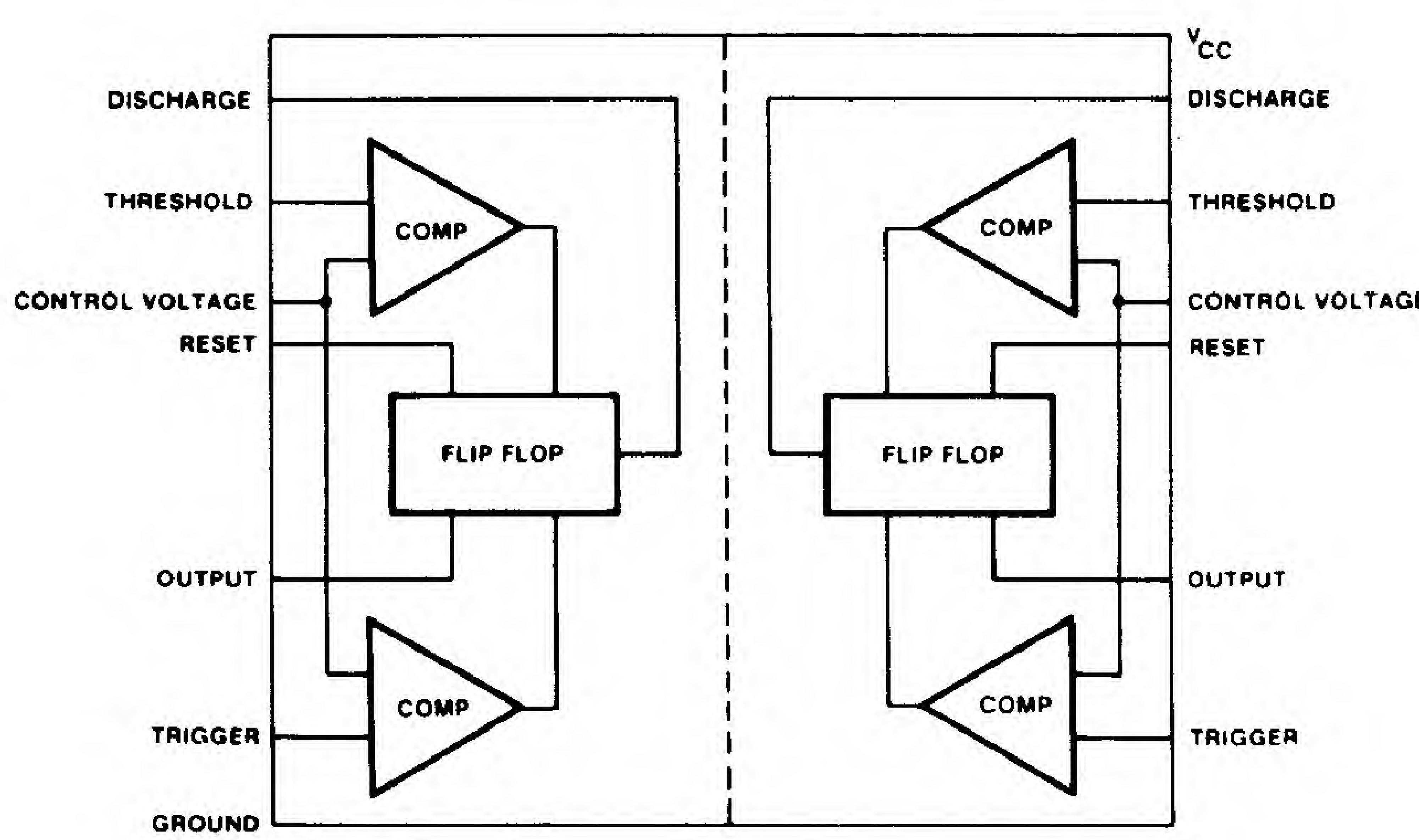




556
DUAL TIMER

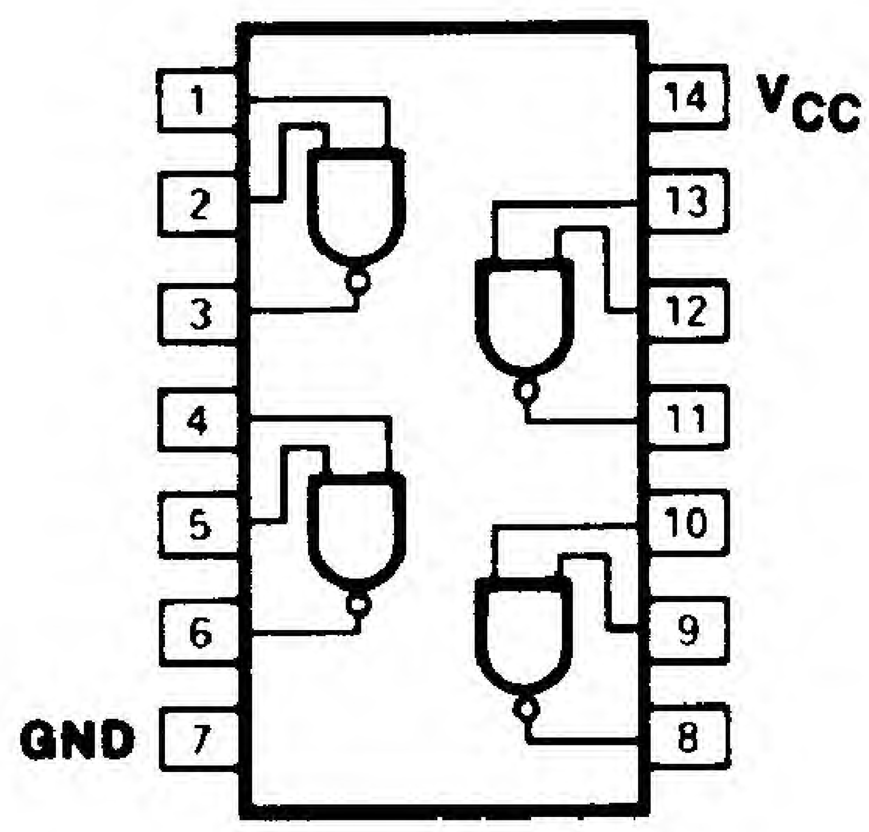
PIN ASSIGNMENTS



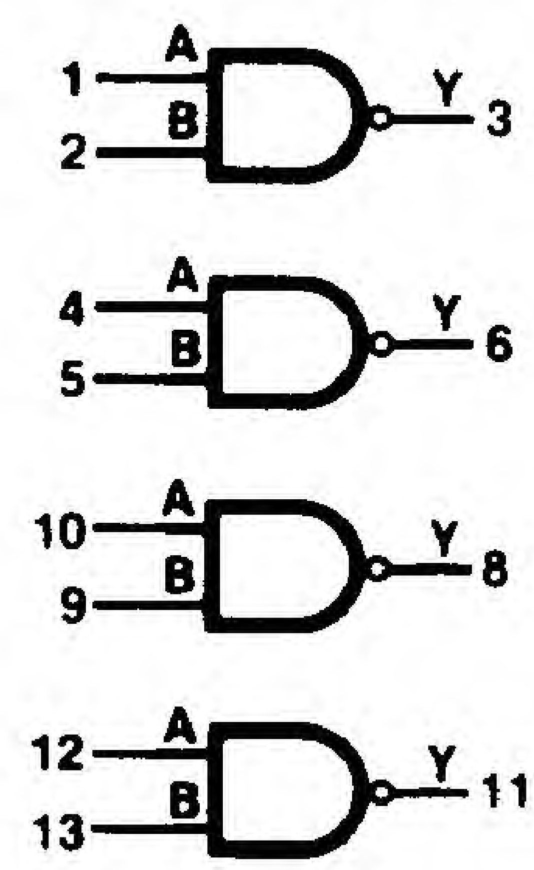


7400 • 74S00 • 74LS00
QUAD 2-INPUT NAND GATE

PIN ASSIGNMENT



LOGIC DIAGRAM



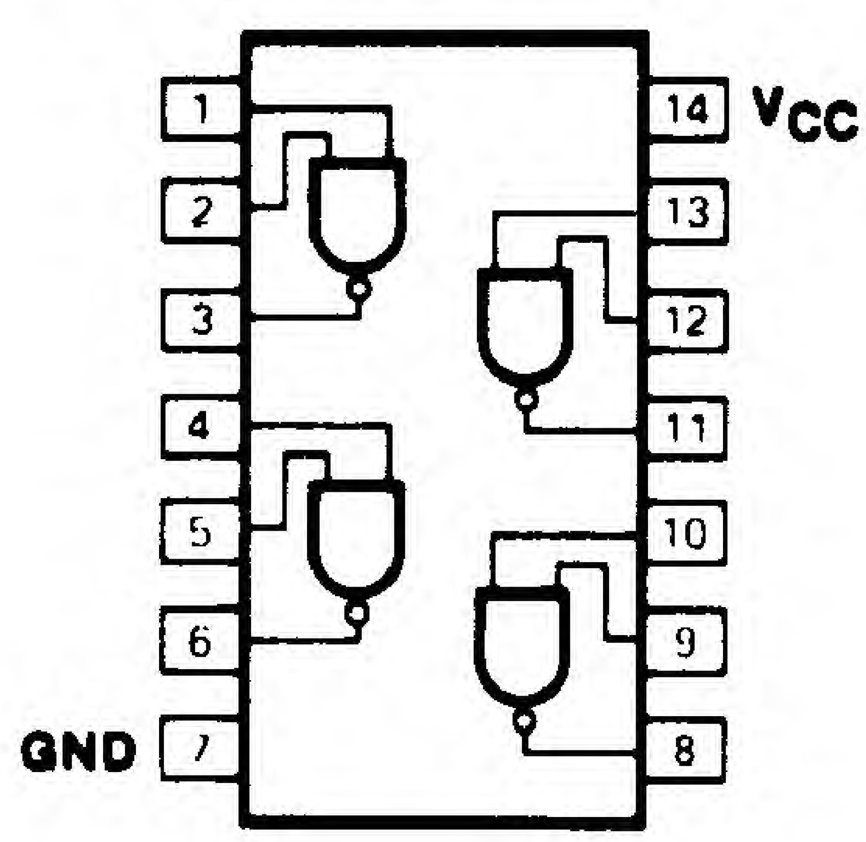
TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

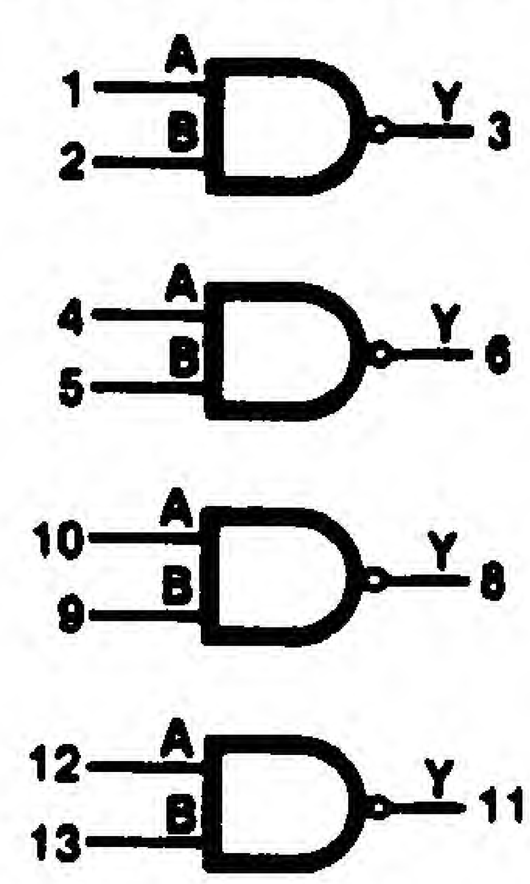
H = HIGH voltage level
L = LOW voltage level

74LS03
QUAD 2-INPUT NAND GATE (OPEN COLLECTOR)

PIN ASSIGNMENT



LOGIC DIAGRAM



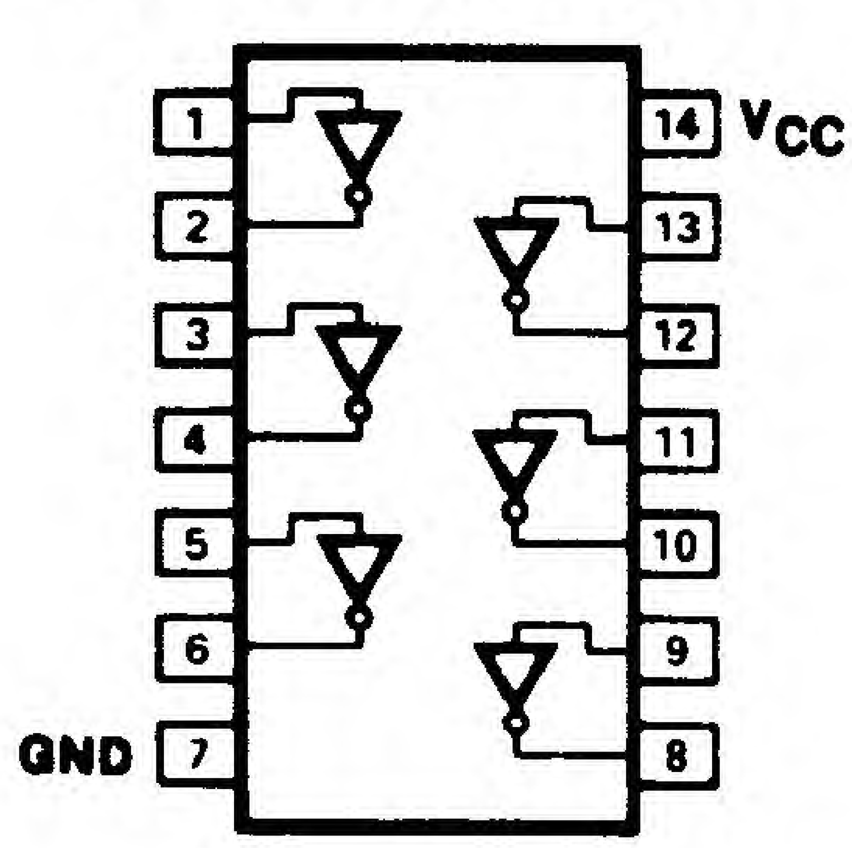
TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

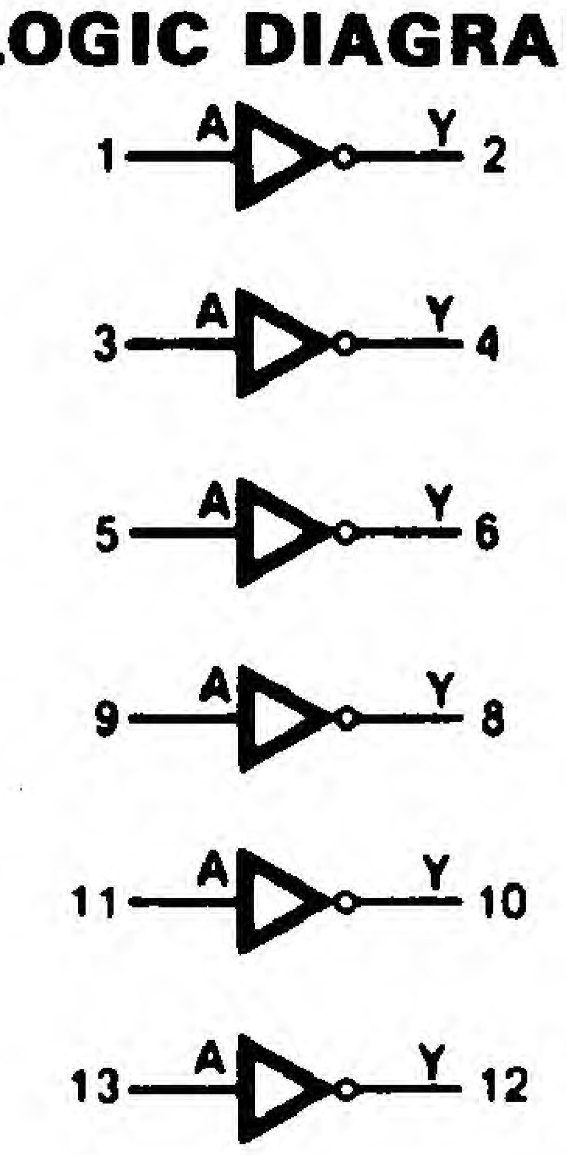
H = HIGH voltage level
L = LOW voltage level

7406
HEX INVERTER BUFFER/DRIVER (OPEN COLLECTOR)

PIN ASSIGNMENT



LOGIC DIAGRAM



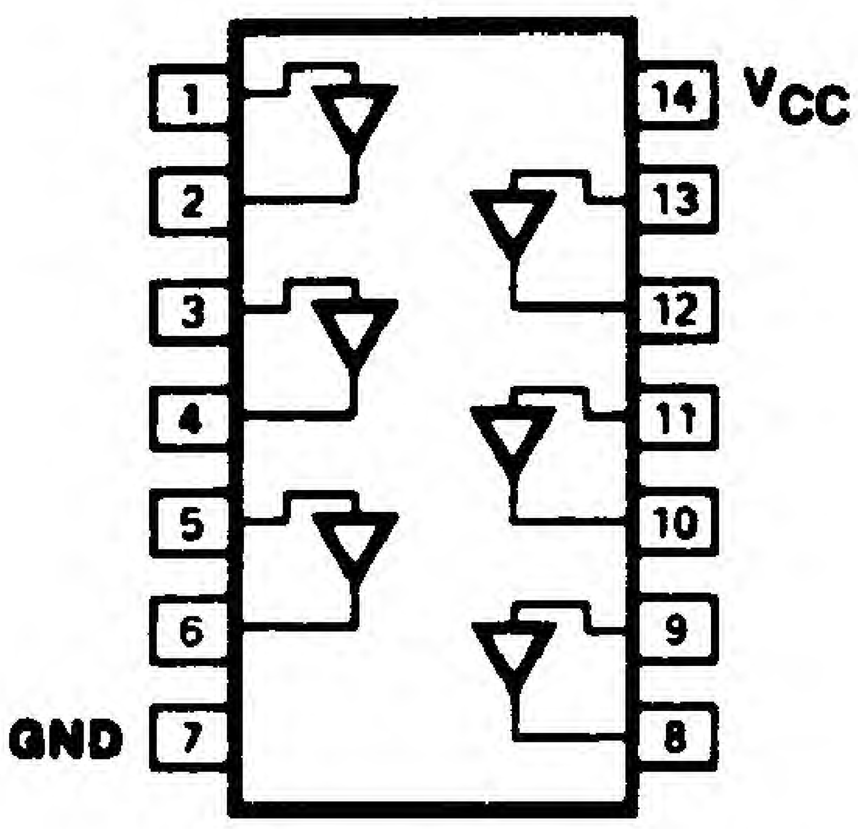
TRUTH TABLE

INPUT	OUTPUT
A	Y
H	L
L	H

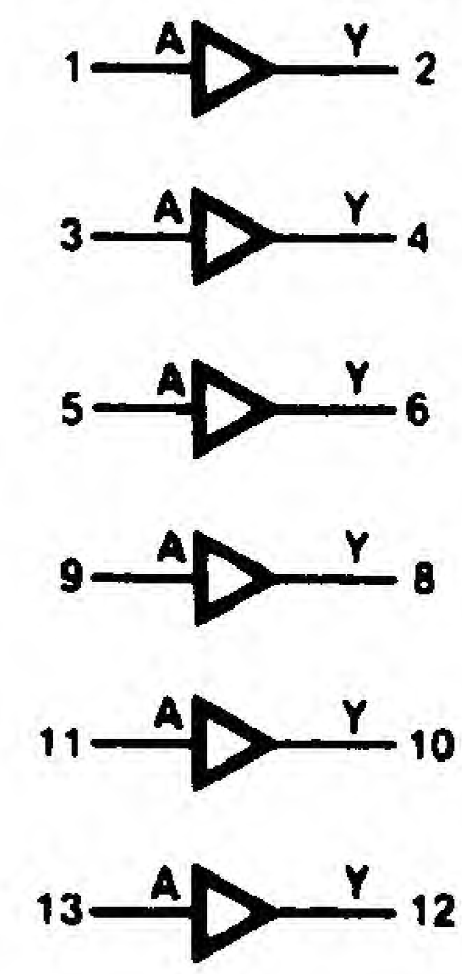
H = HIGH voltage level
L = LOW voltage level

7407
HEX BUFFER/DRIVER (OPEN COLLECTOR)

PIN ASSIGNMENT



LOGIC DIAGRAM



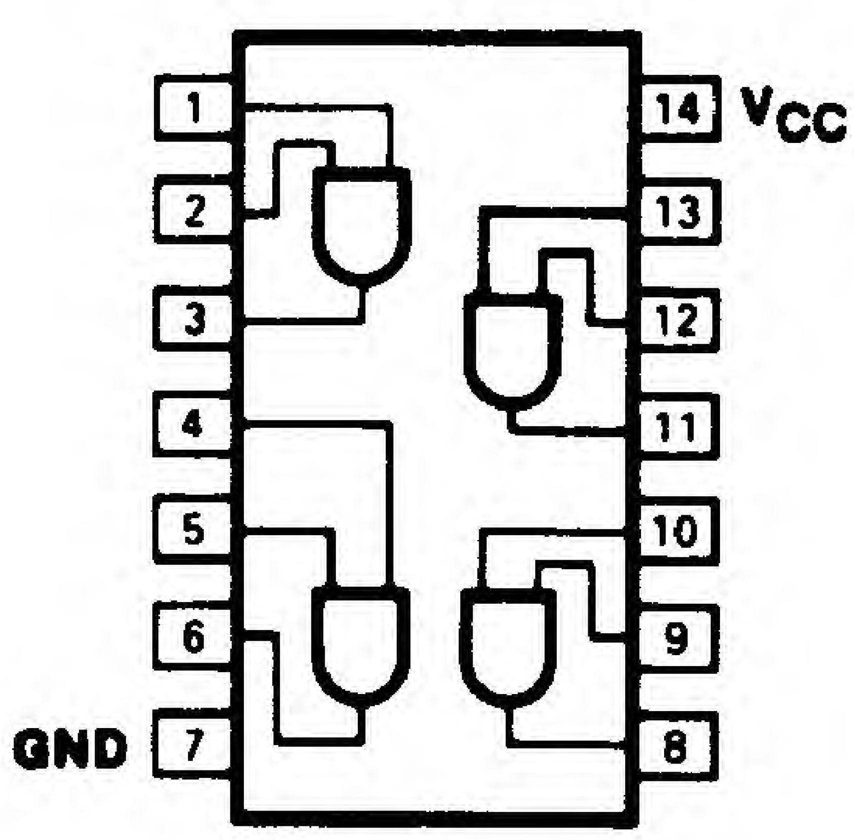
TRUTH TABLE

INPUT	OUTPUT
A	Y
H L	H L

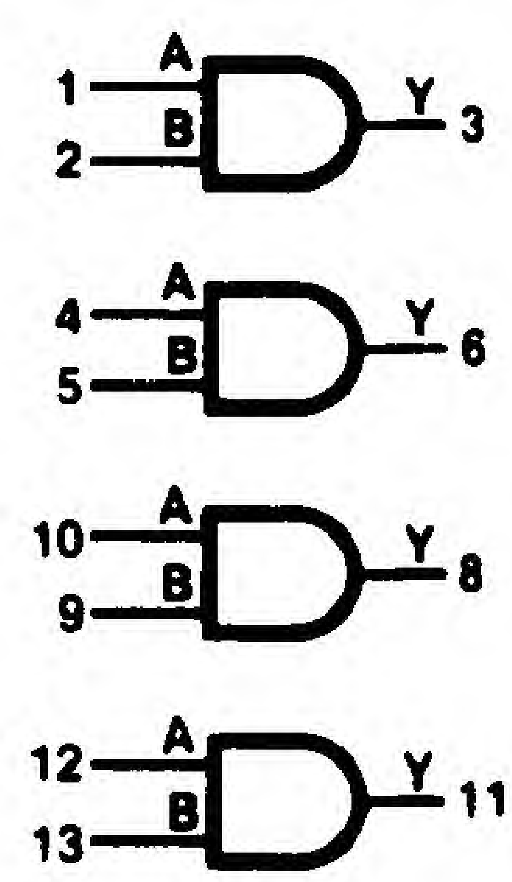
H = HIGH voltage level
L = LOW voltage level

7408 • 74S08 • 74LS08
QUAD 2-INPUT AND GATE

PIN ASSIGNMENT



LOGIC DIAGRAM



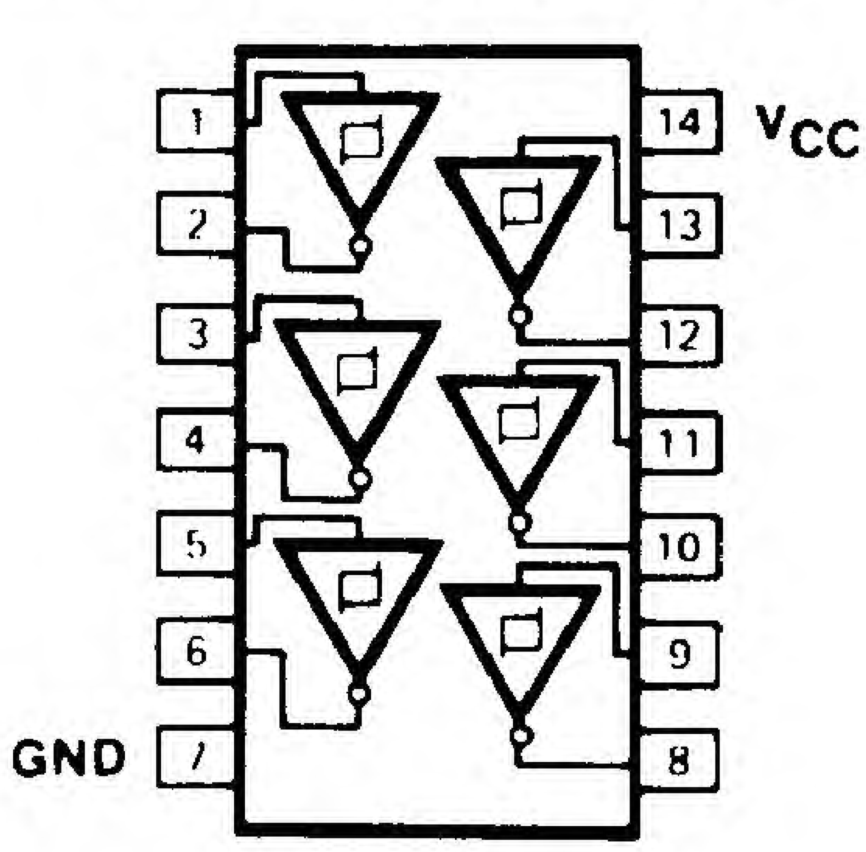
TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L L H H	L H L H	L L L H

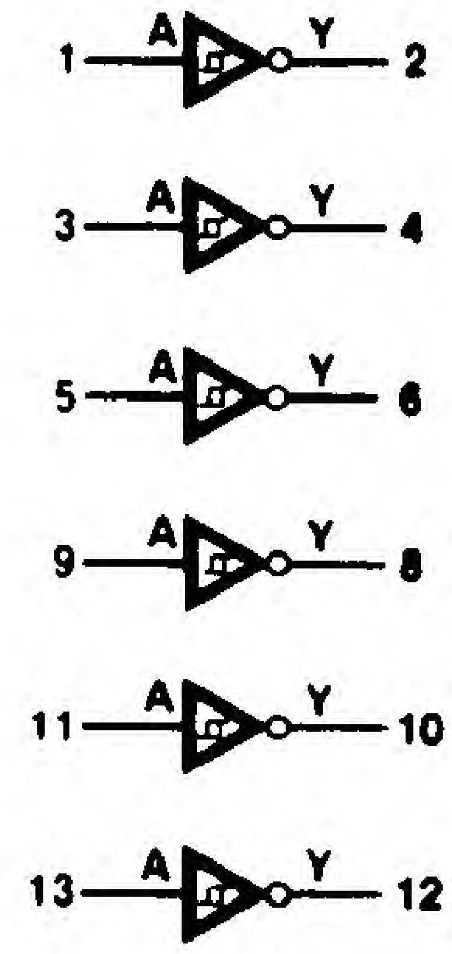
H = HIGH voltage level
L = LOW voltage level

7414 • 74LS14
HEX INVERTER SCHMITT TRIGGER

PIN ASSIGNMENT



LOGIC DIAGRAM



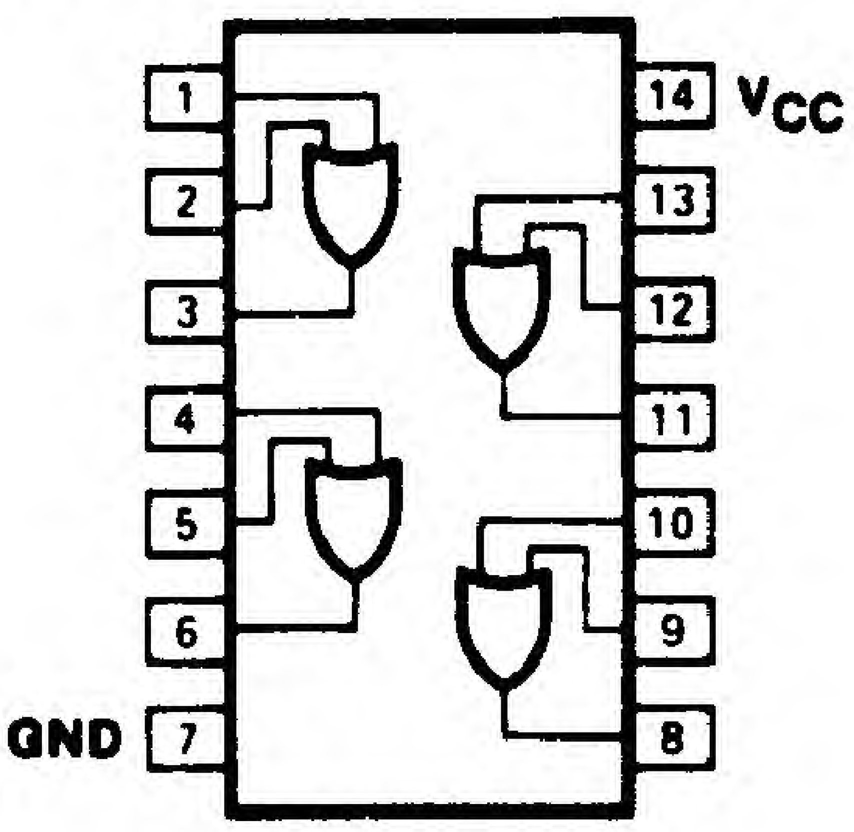
TRUTH TABLE

INPUT	OUTPUT
A	Y
0 1	1 0

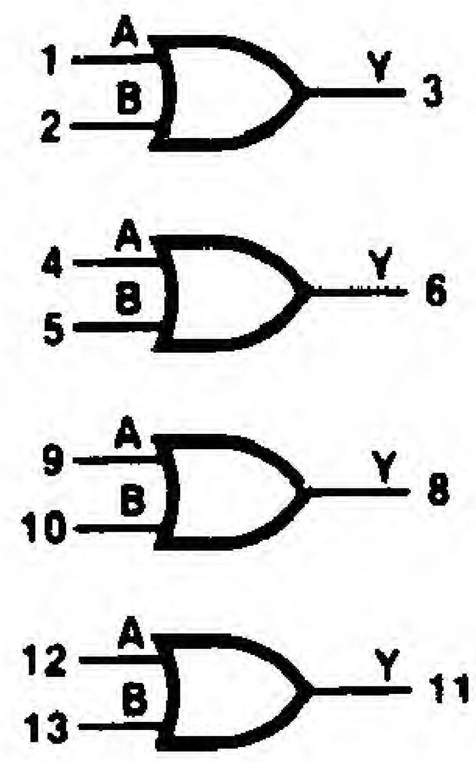
H = HIGH voltage level
L = LOW voltage level

7432 • 74S32 • 74LS32 • 74F32
QUAD 2-INPUT OR GATE

PIN ASSIGNMENT



LOGIC DIAGRAM



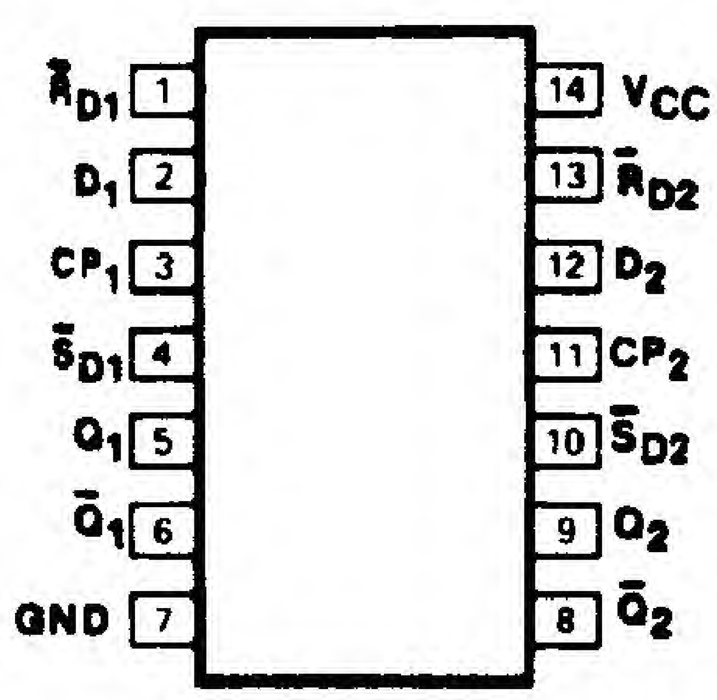
TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

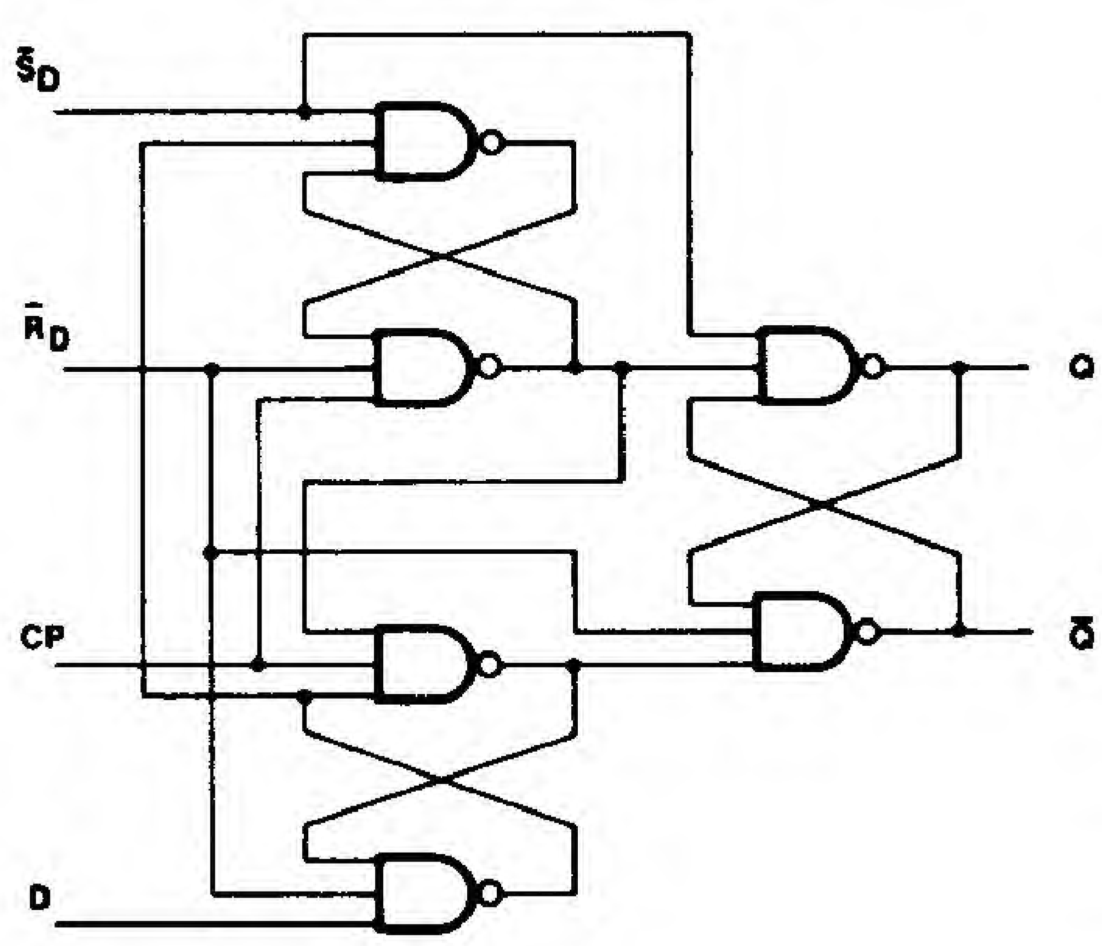
H = HIGH voltage level
L = LOW voltage level

7474 • 74S74 • 74LS74
DUAL D-TYPE FLIP FLOP (POSITIVE EDGE TRIGGERED)

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

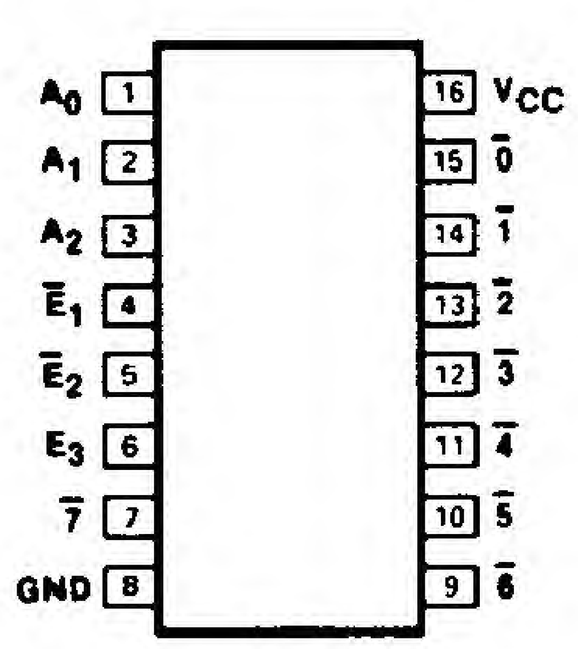
OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined[(a)]	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

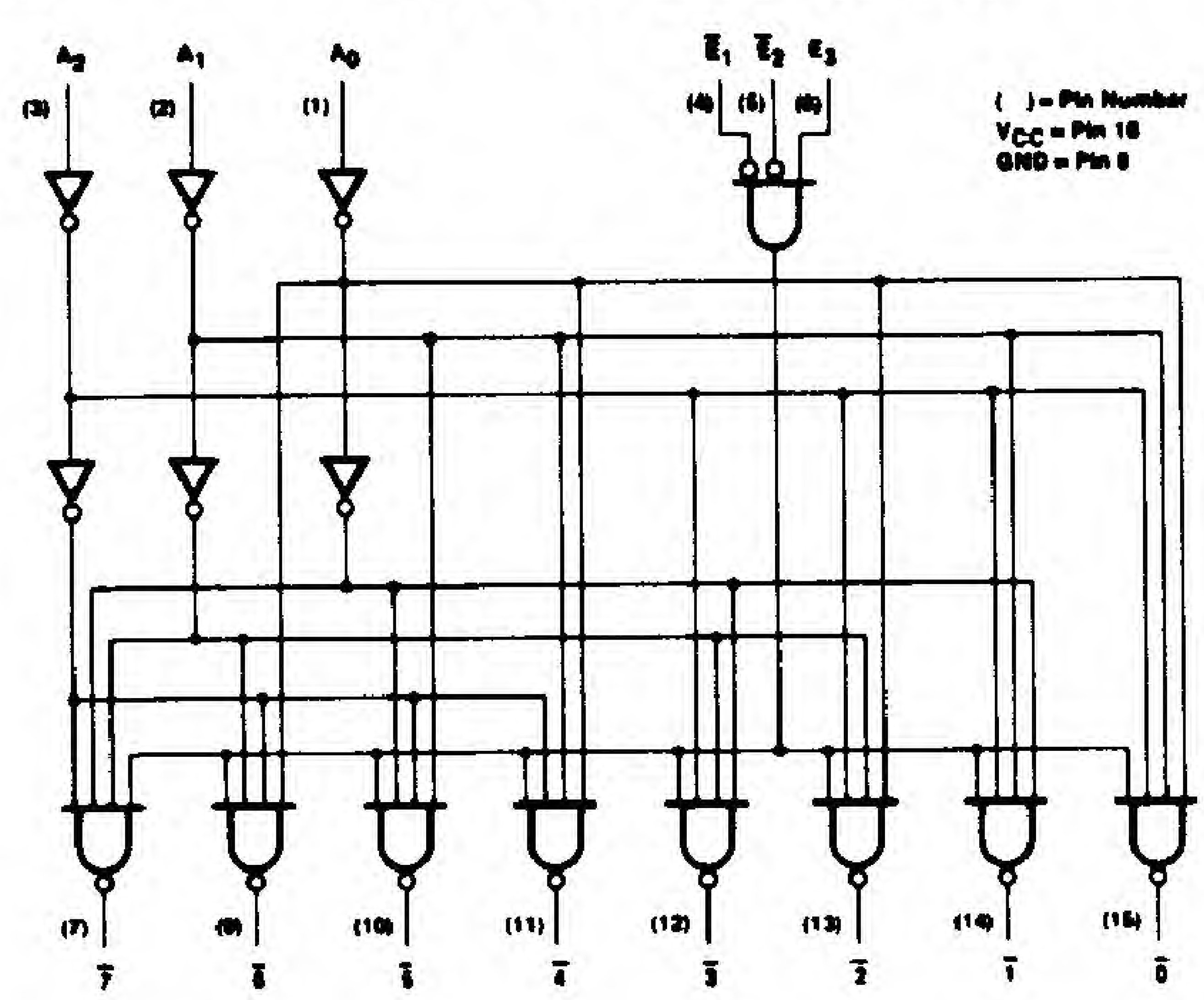
NOTE
(a) Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.

74S138 • 74LS138
DECODER/DEMULTIPLEXER

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

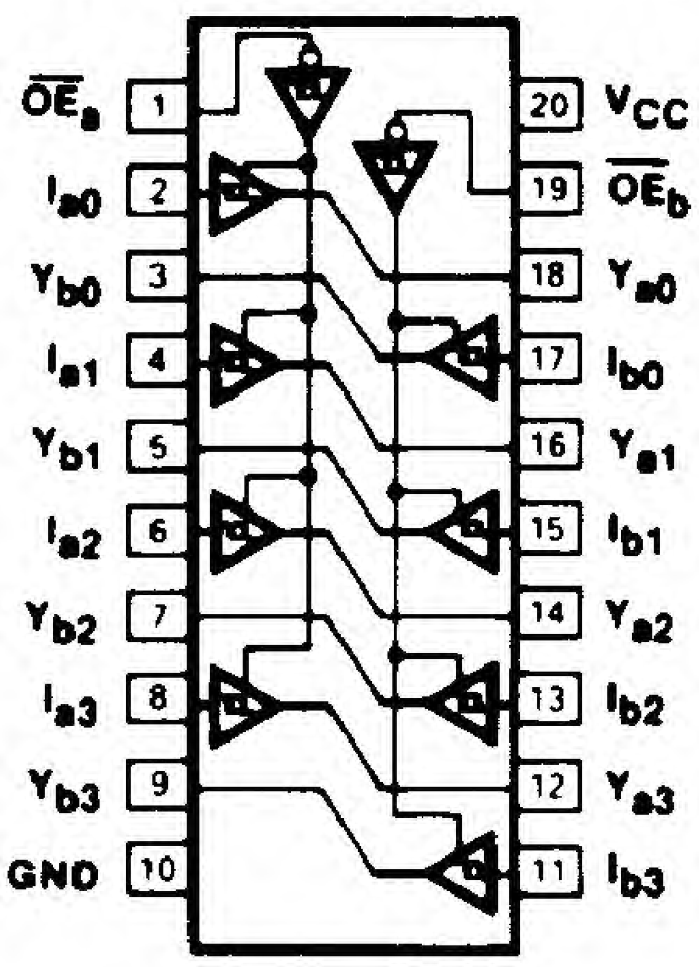
INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES
H = HIGH voltage level
L = LOW voltage level
X = Don't care

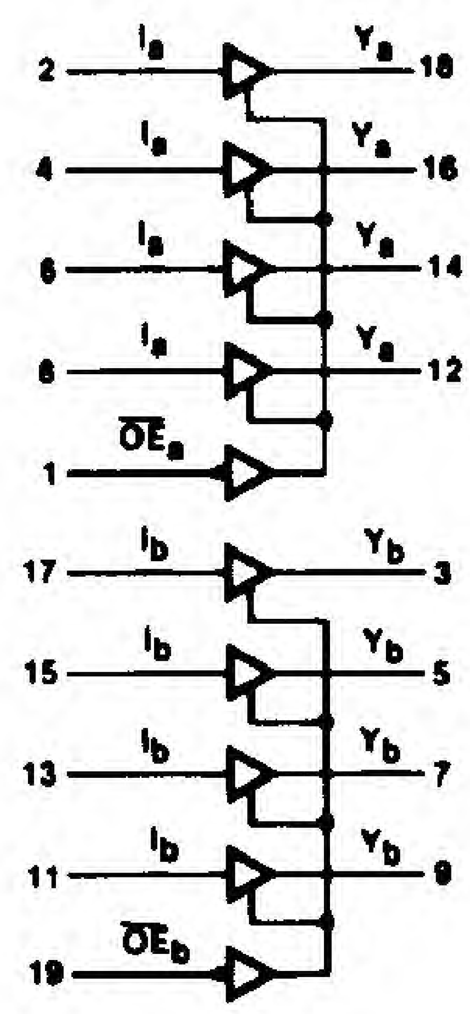
COMMON I.C.'S (Continued)

74S244 • 74LS244
OCTAL 3-STATE BUFFER

PIN ASSIGNMENT



LOGIC DIAGRAM



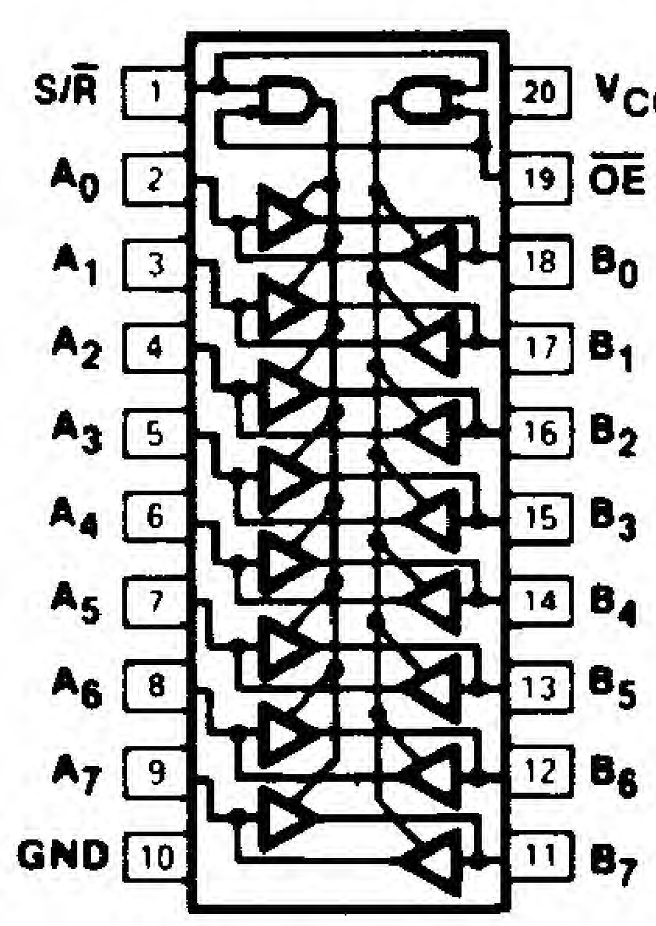
TRUTH TABLE

INPUTS				OUTPUT	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

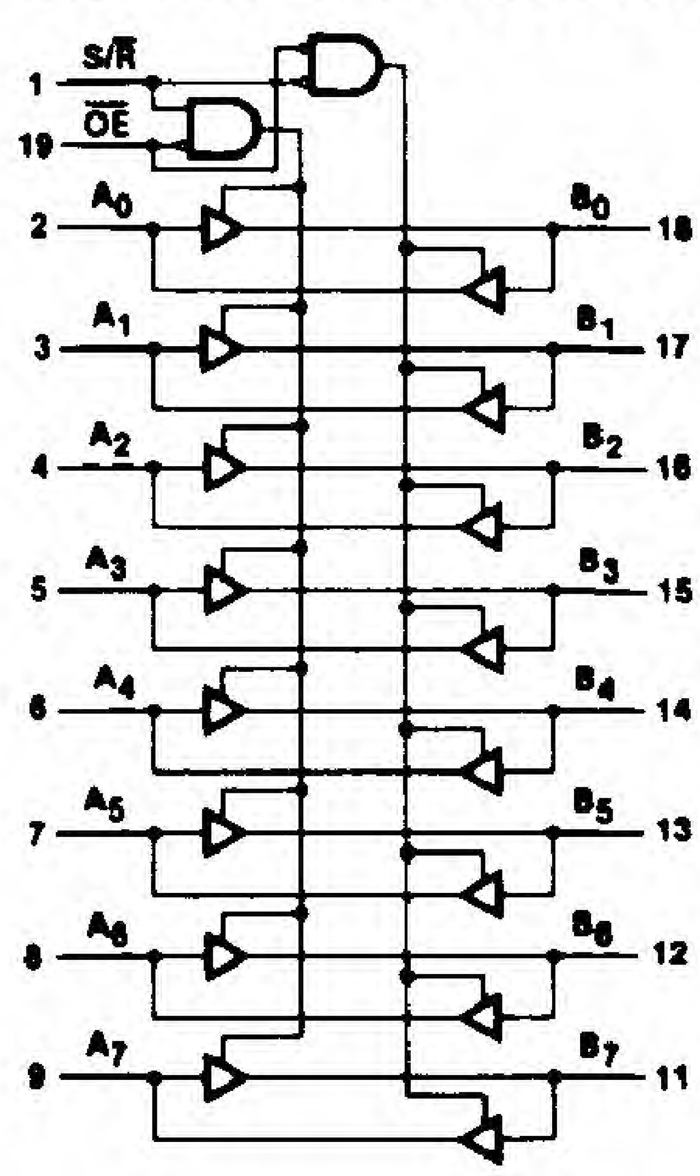
H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = HIGH impedance "off" state

74LS245 • 74F245
OCTAL BUS TRANSCEIVER

PIN ASSIGNMENT



LOGIC DIAGRAM



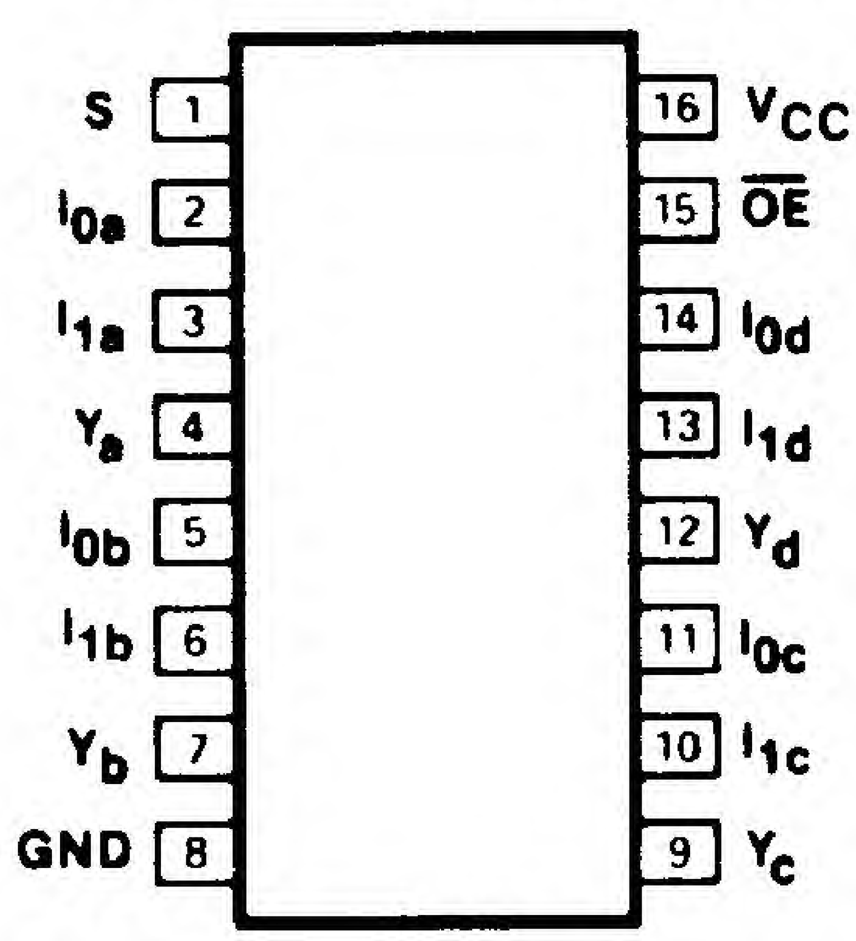
TRUTH TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	S/$\overline{R}$	A_n	B_n
I	I	A = B	INPUTS
L	H	INPUT	B = A
H	X	(Z)	(Z)

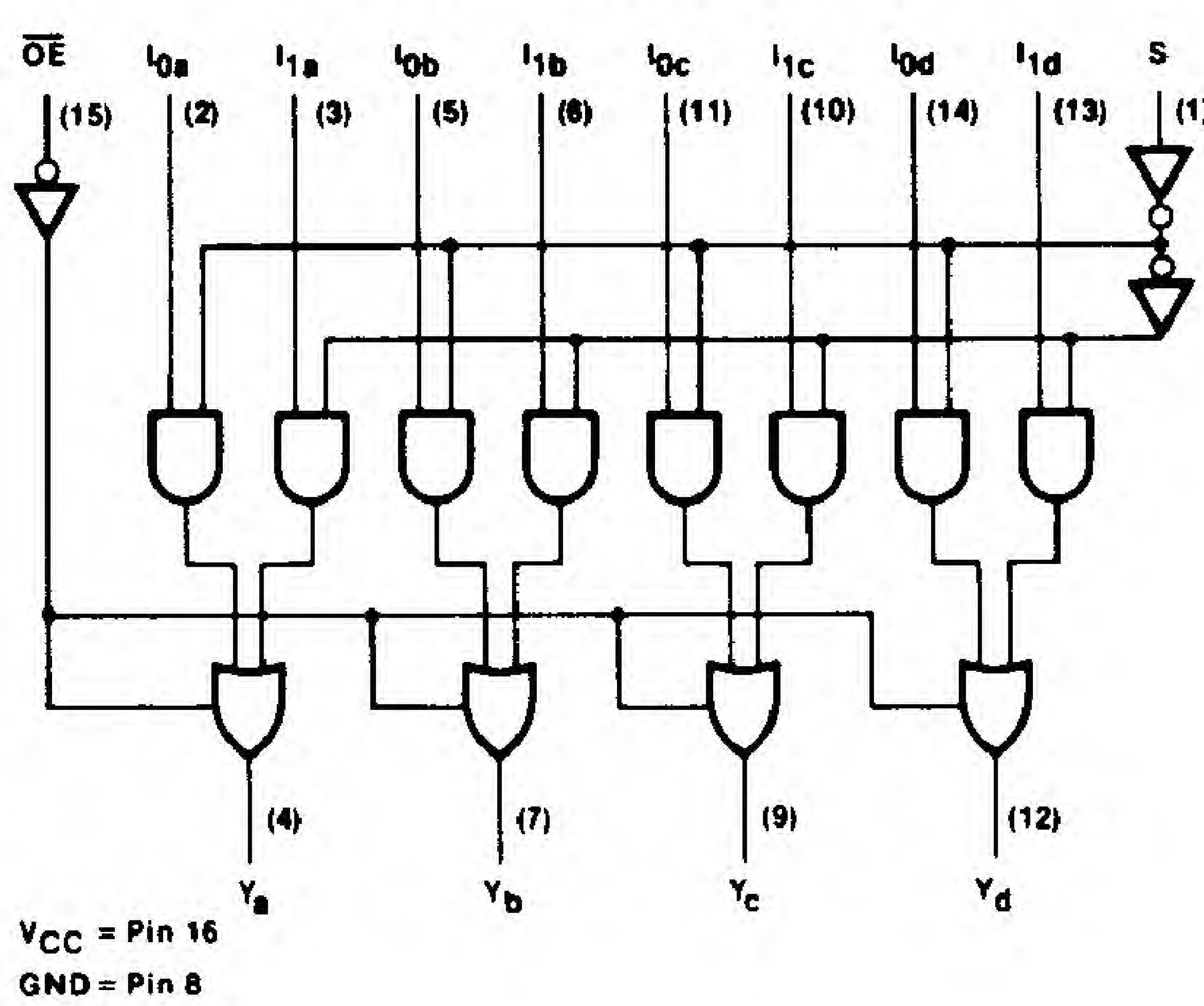
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

72S257 • 74LS257

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

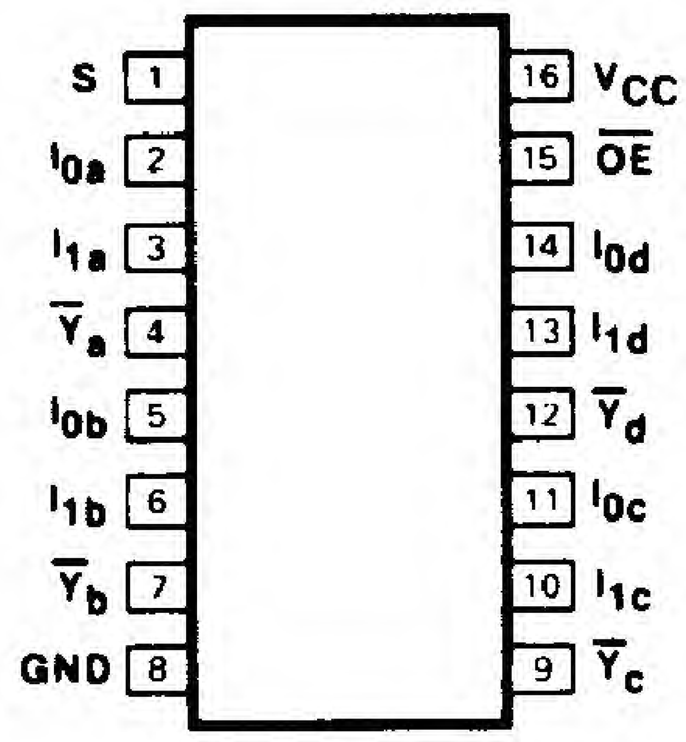
ENABLE	SELECT INPUT
$\overline{OE}$	S
H	X
L	H
L	H
L	L
L	L

INPUTS		OUTPUT
I_0	I_1	Y
X	X	(Z)
X	L	L
X	H	H
L	X	L
H	X	H

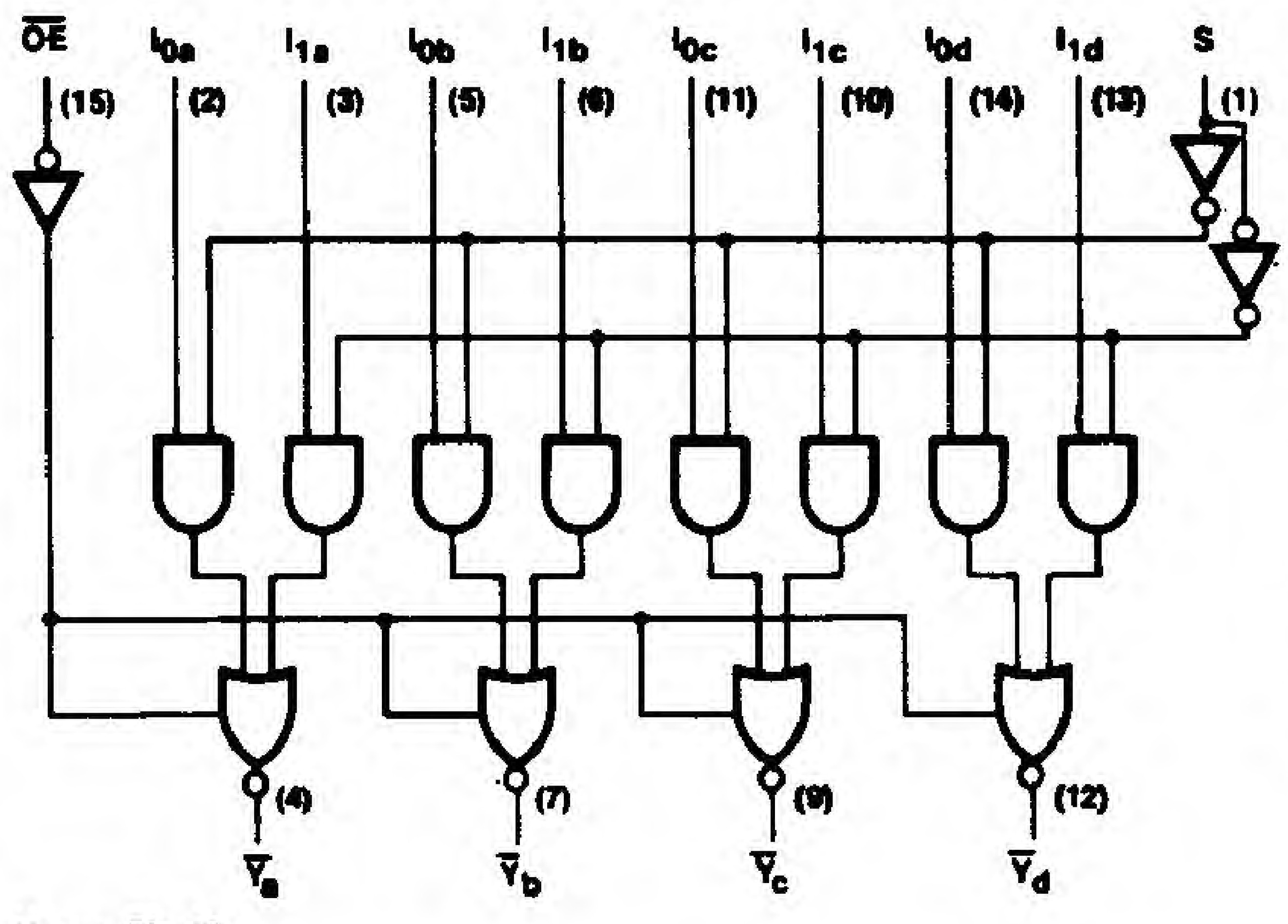
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

72S258 • 74LS258A
QUAD 2:1 MULTIPLEXER (3-STATE)

PIN ASSIGNMENT



LOGIC DIAGRAM



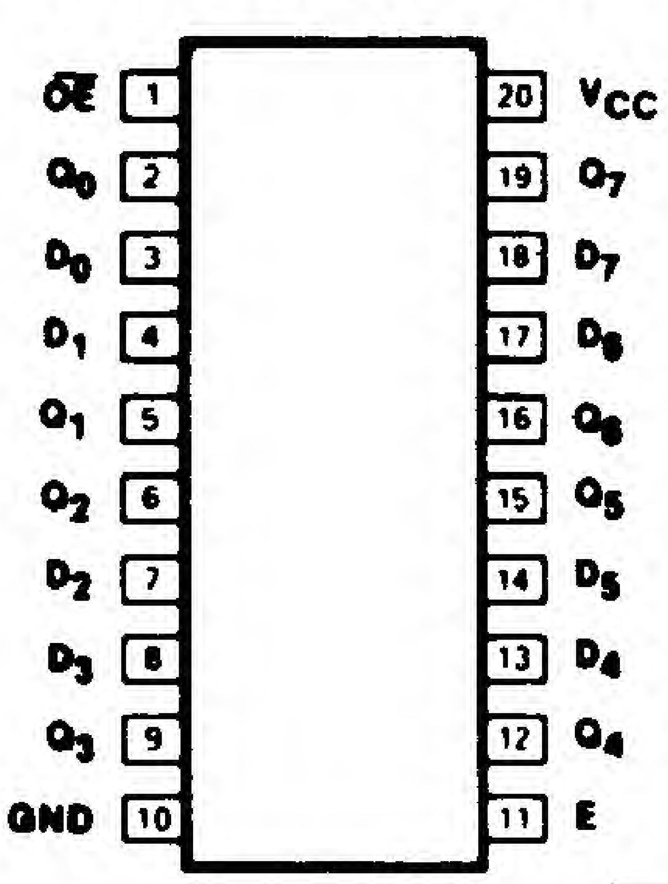
TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

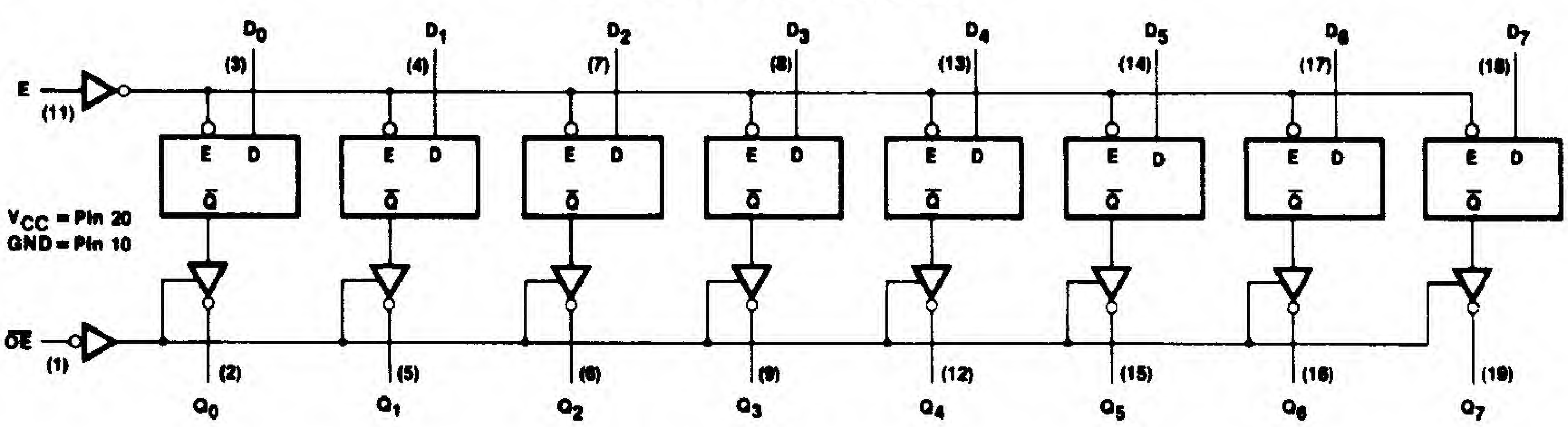
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

74S373 • 74LS373
OCTAL LATCH (3-STATE)

PIN ASSIGNMENT



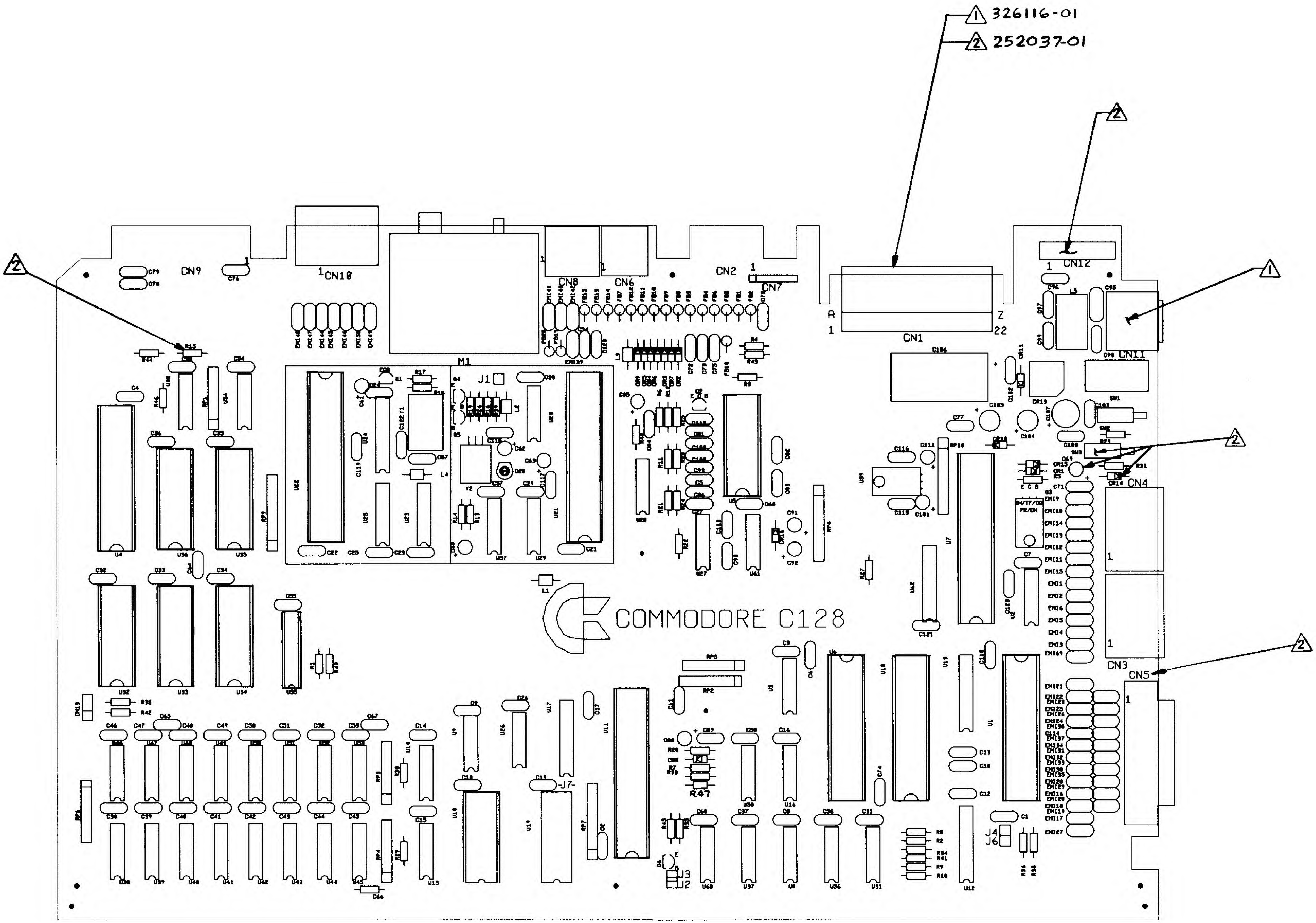
LOGIC DIAGRAM



TRUTH TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0-Q_7
Enable and read register	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition



NOTE :
⚠1 LOW END ONLY
⚠2 HIGH END ONLY

BOARD LAYOUT
PCB ASSY #310379 Revision 6
IDENTIFYING FACTOR: On solder side of board at the EXPANSION BUS, CN1, the artwork #310381 REV. 6 appears.

PARTS LIST
PCB ASSEMBLY #310379
REV. 6

INTEGRATED CIRCUITS

U1	6526 CIA	906108-01
U2	4066	
U3	74LS138	
U4	6526 CIA	906108-01
U5	6581 SID	906112-01
U6	8502 Microprocessor	315020-01
U7	8722-R1 MMU	310389-01
U8	74LS08	
U9	74LS32	
U10	Z80B Microprocessor 6 MHz	906150-02
U11	8721-R3 PLA	315012-01
U12	74LS373	
U13	74LS244	
U14,15	74LS257A	
U16	74LS14	
U17	74ALS373	
U18	ROM 64K 128 Char	390059-01
U19	2016 16K RAM — 200ns	
U20	4066	
U21	8564-R4 VIC	315009-01
U22	8563-R7 CRT Cntrl	315014-01
U23	4416 Dynamic RAM — 150ns	
U24	74LS244	
U25	4416 Dynamic RAM — 150ns	
U26	74LS257A	
U27	556	
U28	8701 Clock Generator	251527-01
U29,30	7406	
U31	74LS00	
U32	ROM 1 — C64 Kern & Basic	251913-01
U33	ROM 2 — Basic $4000	318018-02
U34	ROM 3 — Basic $8000	318019-02
U35	ROM 4 — Kernal $C000	318020-03
U36	ROM Mem Function	Blank
U37	7406	
U38-53	4164 Dynamic RAM — 200ns	
U54	74LS32	
U55	74LS245	
U56	74LS74	
U57	7407	
U58	74LS03	
U59	7812 Regulator 12V, To-220 Case	
U60	7407	
U61	74LS08	
U62	74LS244	

TRANSISTORS

Q1,2	2SC1815
Q3	2SD880
Q4,5,6	2SC1815
Q100	2N4403
Q101	2SC1815
Q102	2N4403

DIODES

CR1	RD6.8EB	Zener 6.8V 400MW
CR2-7	1N914	Sub: IN4148
CR8	1N4371	Zener 2.7V 500MW
CR9	1N914	Sub: IN4148
CR10,11	1N4001	Rect 50V 1A

DIODES (Continued)

CR13	Bridge Rect 100V 2A	251026-01
CR15,16	1N914	
CR100,101	1N914	

RESISTORS — All values in ohms, 1/4W, 5% unless noted otherwise.

R1	68
R2	100
R3	1K
R4	100
R5	470
R6	47K
R7	560
R8	3.3K
R9	10K
R10	3.3K
R11,12	1K
R13,14	330 1W 5%
R16	120
R17	47
R18	82
R19	330 1W 5%
R20	10K
R21	470K
R22	47K
R23	100K
R24	47K
R25	100K
R26	100
R27	4.7K
R28	10K
R29,30	68
R31	100
R32	180
R33,34	10K
R35	100
R36	10K
R38	10K
R39	120
R40	180
R41	680
R42	180
R43,44	3.3K
R45	1.2K
R46	3.3K
R47	1K
R48	10K
R100,101	1K
R102	47K
R103,04	1K
R105	470
R106	1K

RESISTOR PACKS

RP1	1K +/−2%	8 Pin, SIP, Pin 1 Com
RP2	1K 1/8W +/−10%	9 Pin, SIP, Pin 1 Com
RP3,4	33 +/−2%	8 Pin, SIP, Isolated
RP5	3.3K +/−10%	8 Pin, SIP, Pin 1 Com
RP6	1K 1/8W +/−10%	9 Pin, SIP, Pin 1 Com
RP7,8	3.3K	10 Pin, SIP, Pin 1 Com
RP9,10	10K	10 Pin, SIP, Pin 1 Com

PART LIST PCB ASSEMBLY 310379 REV. 6

CAPACITORS — All caps are 25v, +80%, −20% unless noted otherwise.

C1	Cer	.1µF			
C2	Cer	10000pF			
C3-5	Cer	.1F			
C6	Cer	.22µF			
C7-19	Cer	.1µF			
C20	Trim	4-40pF			
C21	Cer	.22µF			
C22	Cer	.1µF			
C23	Cer	.22µF			
C24	Cer	.1µF			
C25	Cer	.22µF			
C26,27	Cer	.1µF			
C28	Cer	.22µF			
C29-37	Cer	.1µF			
C38-53	Cer	.22µF			
C54-58	Cer	.1µF			
C60	Cer	.1µF			
C61-63	Elect Alum	10µF,	16V		
C64,65	Cer	10000pF			
C66	Mylar	.01µF,	250V,	+/−20%	
C67	Cer	10000µF			
C68	Cer	.1µF			
C69	Elect Alum	10µF,	16V		
C70,71	Cer	.1µF			
C72,73	Cer	470pF,	50V,	10%	
C74	Cer	10000pF			
C75	Cer	470pF,	50V,	10%	
C76	Cer	.1µF			
C77	Cer	10000pF			
C78,C79	Cer	1000pF,	50V,	10%	
C80	Elect	2.2µF,	25V		
C81	Cer	1000pF,	50V,	10%	
C82,83	Cer	470pF,	50V,	10%	
C84	Cer	220pF,	50V,	10%	
C85	Elect Alum	10µF,	16V		
C86	Cer	.1µF			
C87	Cer	.22µF			
C88	Elect Alum	10µF,	16V		
C89	Cer	51pF,	50V,	+/−5%	
C90	Cer	360pF,	50V,	+/−5%	
C91	Elect	1µF,	16V		
C92	Elect Alum	10µF,	16V		
C93	Cer	.1µF			
C94	Cer	.22µF			
C95	Cer Mono	.22µF,	100V,	+80%, −20%	
C96-99	Cer	.22µF,	50V		
C100	Cer	.1µF			
C101	Elect	10µF,	35V,	+/−20%	
C102	Cer	.1µF			
C103	Cer	10000pF			
C104	Elect	220µF,	50V		

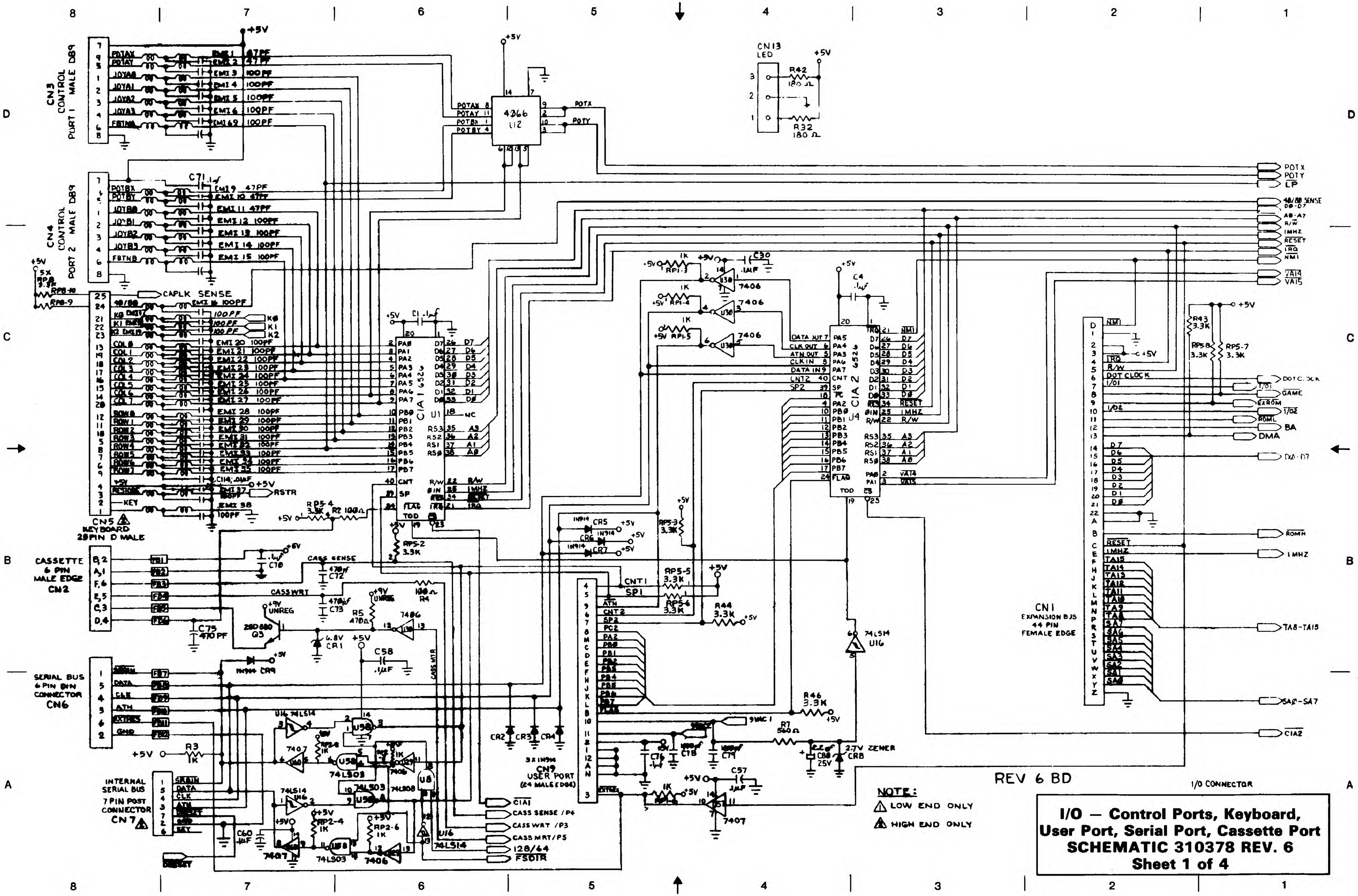
CAPACITORS (Continued)

C105	Elect	330µF,	50V,	+/−20%
C106	Elect	1000µF,	25V	
C107	Elect	100µF,	16V	
C108,9	Cer	1800pF,	50V	10%
C110	Cer	10000pF		
C111	Elect Alum	10µF,	16V	
C112	Cer	470pF,	50V,	10%
C113,14	Cer	10000pF		
C115,16	Cer	.1µF		
C117-23	Cer	10000pF		
C124	Cer	.1µF,	16V	

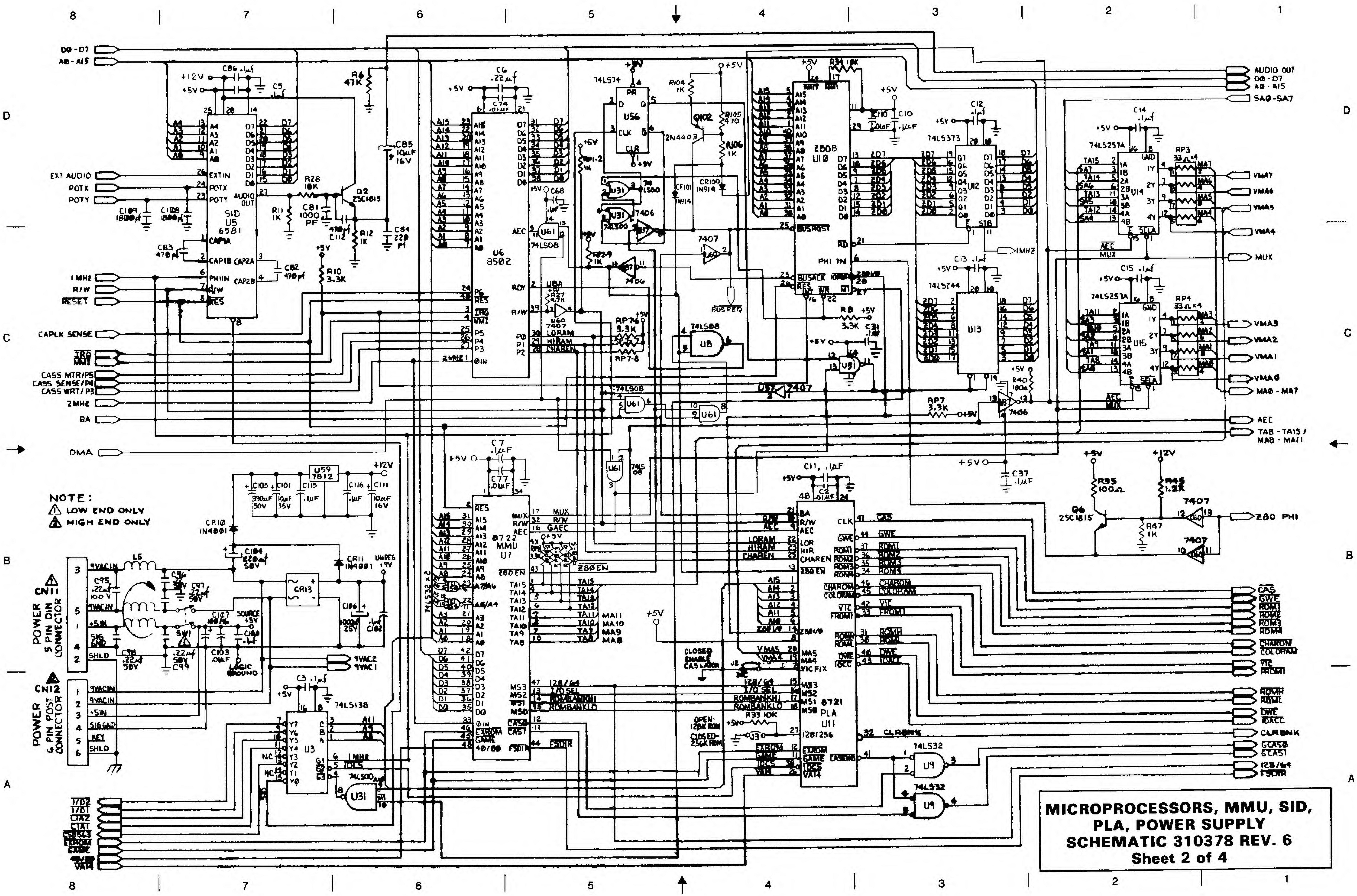
MISCELLANEOUS

Y1	16 MHz Clock Oscillator	325566-01
Y2	14.31818 Crystal	251467-01
L1-4	Inductor 2.2µH	
L5	Line Filter Assy	251878-01
FB1-15, 18-20	Ferrite Beads	
EMI1,2	EMI Filter	47pF
EMI3-6	EMI Filter	100pF
EMI9-11	EMI Filter	47pF
EMI12-35, 37,38	EMI Filter	100pF
EMI39	EMI Filter	270pF
EMI40-42	EMI Filter	100pF
EMI44-50	Ferrite Bead	
EMI69	EMI Filter	100pF
M1	Modulator	251917-01
SW1	Rocker Switch	252182-01
SW2	Push BT SPDT	251260-01
CN1	RT Angle Card Edge	906100-02
CN3,4	Mini D Cnnct Joy1,2	251057-01
CN6,7	6 Pin Din Serial Cnnct Shld	252166-01
CN8	8 Pin Din Video Cnnct Shld	252168-01
CN10	D Cnnct 9 Pin Fem Rgbi	252024-01
CN11	5 Pin Square Din Shielded	252167-01
CN13	3 Pin Header .1 Center	
	Shield Box	326265-02
	Shield Cap	310407-01

QUICK REFERENCE

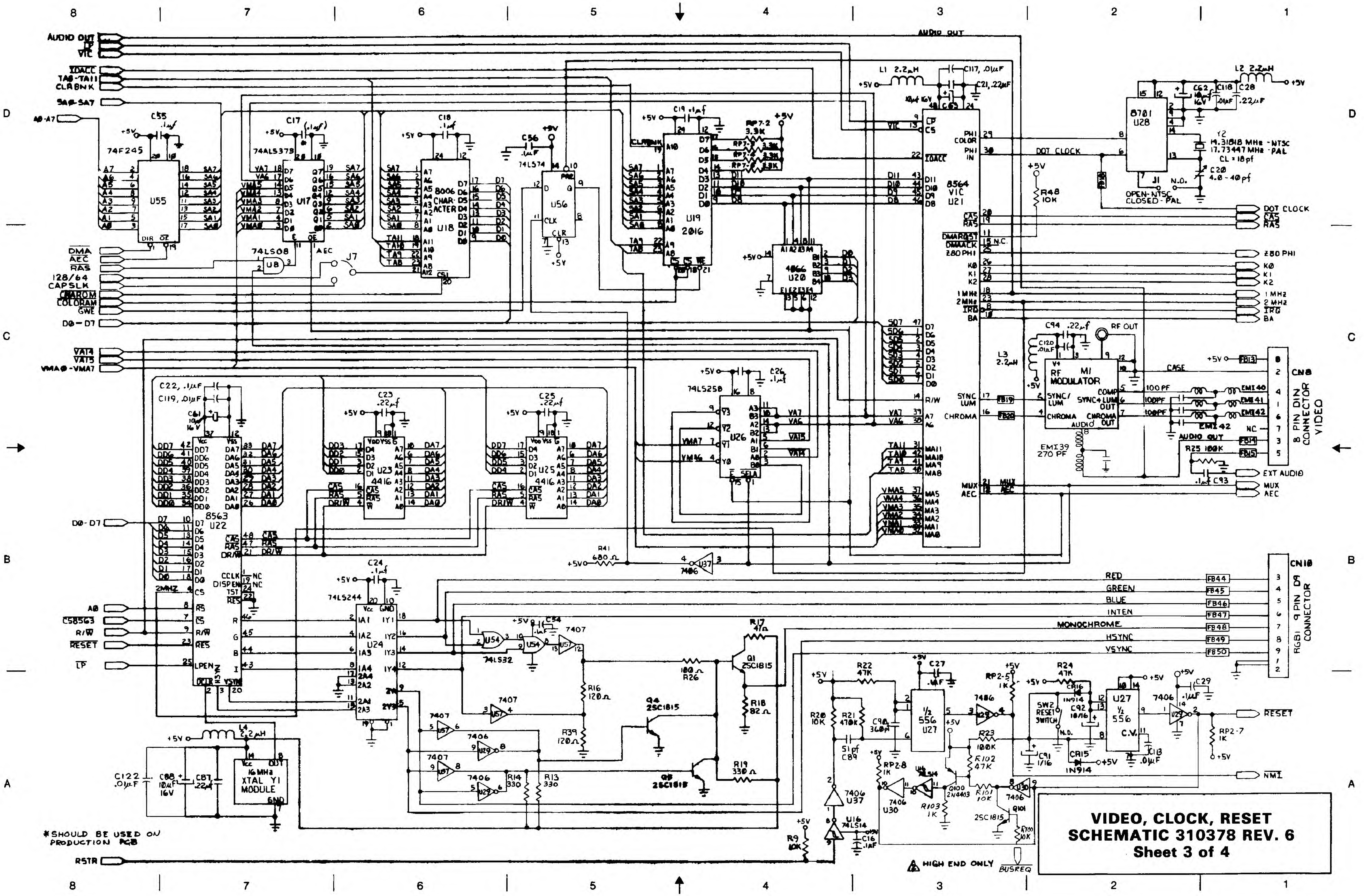

CN3 CONTROL PORT 1 MALE DB9
CN4 CONTROL PORT 2 MALE DB9
CN5 KEYBOARD 25PIN D MALE
CASSETTE 6 PIN MALE EDGE CN2
SERIAL BUS 6 PIN DIN CONNECTOR CN6
INTERNAL SERIAL BUS 7 PIN POST CONNECTOR CN 7
CN13 LED
CIA 1 6526 U1
CIA 2 6526 U4
4066 U12
CN9 USER PORT (24 MALE EDGE)
CN1 EXPANSION BUS 44 PIN FEMALE EDGE
I/O CONNECTOR
REV 6 BD
NOTE:
LOW END ONLY
HIGH END ONLY
I/O — Control Ports, Keyboard, User Port, Serial Port, Cassette Port
SCHEMATIC 310378 REV. 6
Sheet 1 of 4

QUICK REFERENCE



MICROPROCESSORS, MMU, SID, PLA, POWER SUPPLY SCHEMATIC 310378 REV. 6
Sheet 2 of 4

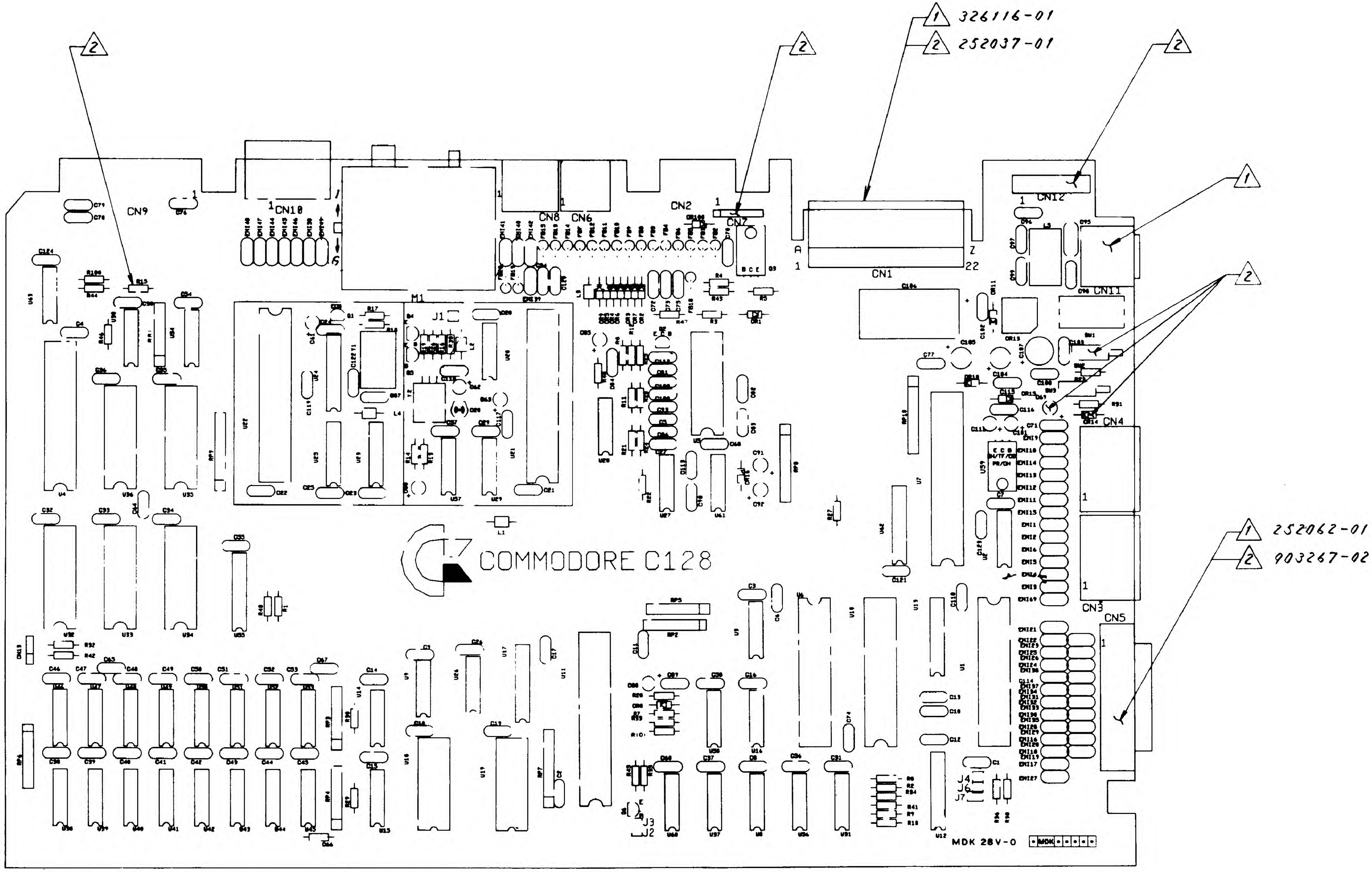
QUICK REFERENCE



VIDEO, CLOCK, RESET SCHEMATIC 310378 REV. 6
Sheet 3 of 4

QUICK REFERENCE

RAM, ROM
SCHEMATIC 310378 REV. 6
Sheet 4 of 4



NOTE :

1 : LOW END ONLY

2 : HIGH END ONLY

BOARD LAYOUT
PCB ASSY #310379 Revision 7
IDENTIFYING FACTOR: On solder side of board at the EXPANSION BUS, CN1, the artwork #310381 REV. 7 appears.

PARTS LIST
PCB ASSEMBLY #310379
REV. 7

INTEGRATED CIRCUITS

U1	6526 CIA	906108-01
U2	4066	
U3	74LS138	
U4	6526 CIA	906108-01
U5	6581 SID	906112-01
U6	8502 Microprocessor	315020-01
U7	8722-R1 MMU	310389-01
U8	74LS08	
U9	74F32	
U10	Z80B Microprocessor 6 MHz	906150-02
U11	8721-R3 PLA	315012-01
U12	74LS373	
U13	74LS244	
U14,15	74LS257A	
U16	74LS14	
U17	74ALS373	
U18	ROM 64K 128 Char	390059-01
U19	2016 16K RAM — 200ns	
U20	4066	
U21	8564-R4 VIC	315009-01
U22	8563-R7 CRT Cntrl	315014-01
U23	4416 Dynamic RAM — 150ns	
U24	74LS244	
U25	4416 Dynamic RAM — 150ns	
U26	74LS257A	
U27	556	
U28	8701C Clock Generator	251527-03
U29,30	7406	
U31	74LS00	
U32	ROM 1 — C64 Kern & Basic	251913-01
U33	ROM 2 — Basic $4000	318018-02
U34	ROM 3 — Basic $8000	318019-02
U35	ROM 4 — Kernal $C000	318020-03
U36	ROM Mem Function	Blank
U37	7406	
U38-53	4164 Dynamic RAM — 150ns	
U54	74LS32	
U55	74F245	
U56	74LS74	
U57	7407	
U58	74LS03	
U59	7812 Regulator 12V, TO-220 CASE	
U60	7407	
U61	74LS08	
U62	74LS244	
U63	7406	

TRANSISTORS

Q1,2	2SC1815
Q3	2SD880
Q4,5,6	2SC1815

DIODES

CR1	RD6.8EB	Zener 6.8V 400MW
CR2-7	1N914	Sub: IN4148
CR8	1N4371	Zener 2.7V 500MW
CR9	1N914	Sub: IN4148
CR10,11	1N4001	Rect 50V 1A

DIODES (Continued)

CR13	Bridge Rect 100V 2A	251026-01
CR15,16	1N914	Sub: IN4148
CR100	1N914	Sub: IN4148

RESISTORS — All values in ohms, 1/4W, 5% unless noted otherwise.

R1	68
R2	100
R3	1K
R4	100
R5	470
R6	47K
R7	560
R8	3.3K
R9	10K
R10	3.3K
R11,12	1K
R13,14	330 1W 5%
R16	120
R17	47
R18	82
R19	330 1W 5%
R20	10K
R21	470K
R22	47K
R23	100K
R24	47K
R25	100K
R26	100
R27	4.7K
R28	10K
R29,30	68
R31	100
R32	180
R33,34	10K
R35	100
R36	10K
R38	10K
R39	120
R40	180
R41	680
R42	180
R43,44	3.3K
R45	1.2K
R46	3.3K
R47	1K
R48	10K
R100,101	1K
R102	68

RESISTOR PACKS

RP1	1K +/−2%	8 Pin, SIP, Pin 1 Com
RP2	1K 1/8W +/−10%	9 Pin, SIP, Pin 1 Com
RP3,4	33 +/−2%	8 Pin, SIP, Isolated
RP5	3.3K +/−10%	8 Pin, SIP, Pin 1 Com
RP6	1K 1/8W +/−10%	9 Pin, SIP, Pin 1 Com
RP7,8	3.3K	10 Pin, SIP, Pin 1 Com
RP9,10	10K	10 Pin, SIP, Pin 1 Com

PART LIST PCB ASSEMBLY 310379 REV. 7

CAPACITORS — All caps are 25v, +80%, −20% unless noted otherwise.

C1	Cer	.1µF		
C2	Cer	.01µF		
C3-5	Cer	.1F		
C6	Cer	.22µF		
C7-19	Cer	.1µF		
C20	Trim	4-40pF		
C21	Cer	.22µF		
C22	Cer	.1µF		
C23	Cer	.22µF		
C24	Cer	.1µF		
C25	Cer	.22µF		
C26,27	Cer	.1µF		
C28	Cer	.22µF		
C29-37	Cer	.1µF		
C38-53	Cer	.22µF		
C54-58	Cer	.1µF		
C50	Cer	.1µF		
C61-62	Elect Alum	10µF,	16V	
C63	Elect Alum	100µF,	6.3V	
C64,65	Cer	.01µF		
C66	Cer	.01µF,	25V	A
C67	Cer	.01µF		
C68	Cer	.1µF		
C70,71	Cer	.1µF		
C72,73	Cer	470pF,	50V,	10%
C74	Cer	.01µF		
C75	Cer	470pF,	50V,	10%
C76	Cer	.1µF		
C77	Cer	.01µF		
C78,C79	Cer	1000pF,	50V,	10%
C80	Elect	2.2µF,	25V	
C81	Cer	1000pF,	50V,	10%
C82,83	Cer	470pF,	50V,	10%
C84	Cer	220pF,	50V,	10%
C85	Elect Alum	10µF,	16V	
C86	Cer	.1µF		
C87	Cer	.22µF		
C88	Elect Alum	10µF,	16V	
C89	Cer	51pF,	50V,	+/−5%
C90	Cer	360pF,	50V,	+/−5%
C91	Elect	1µF,	50V	
C92	Elect Alum	10µF,	16V	
C93	Cer	.1µF		
C94	Cer	.22µF		
C95	Cer Mono	.22µF,	100V,	+80%, −20%
C96-99	Cer	.1µF,	16V	
C100	Cer	.1µF		
C101	Elect	10µF,	35V,	+/−20%
C102	Cer	.1µF		
C103	Cer	.01µF		
C104	Elect	220µF,	50V	

CAPACITORS (Continued)

C105	Elect	330µF,	50V,	+/−20%
C106	Elect	1000µF,	25V	
C107	Elect	100µF,	16V	
C108,9	Cer	.01µF		
C110	Cer	.01µF		
C111	Elect Alum	10µF,	16V	
C112	Cer	470pF,	50V,	10%
C113,14	Cer	.01µF		
C115,16	Cer	.1µF		
C117-23	Cer	.01µF		
C124	Cer	.1µF,	16V	
C125,126	Cer	.01µF		

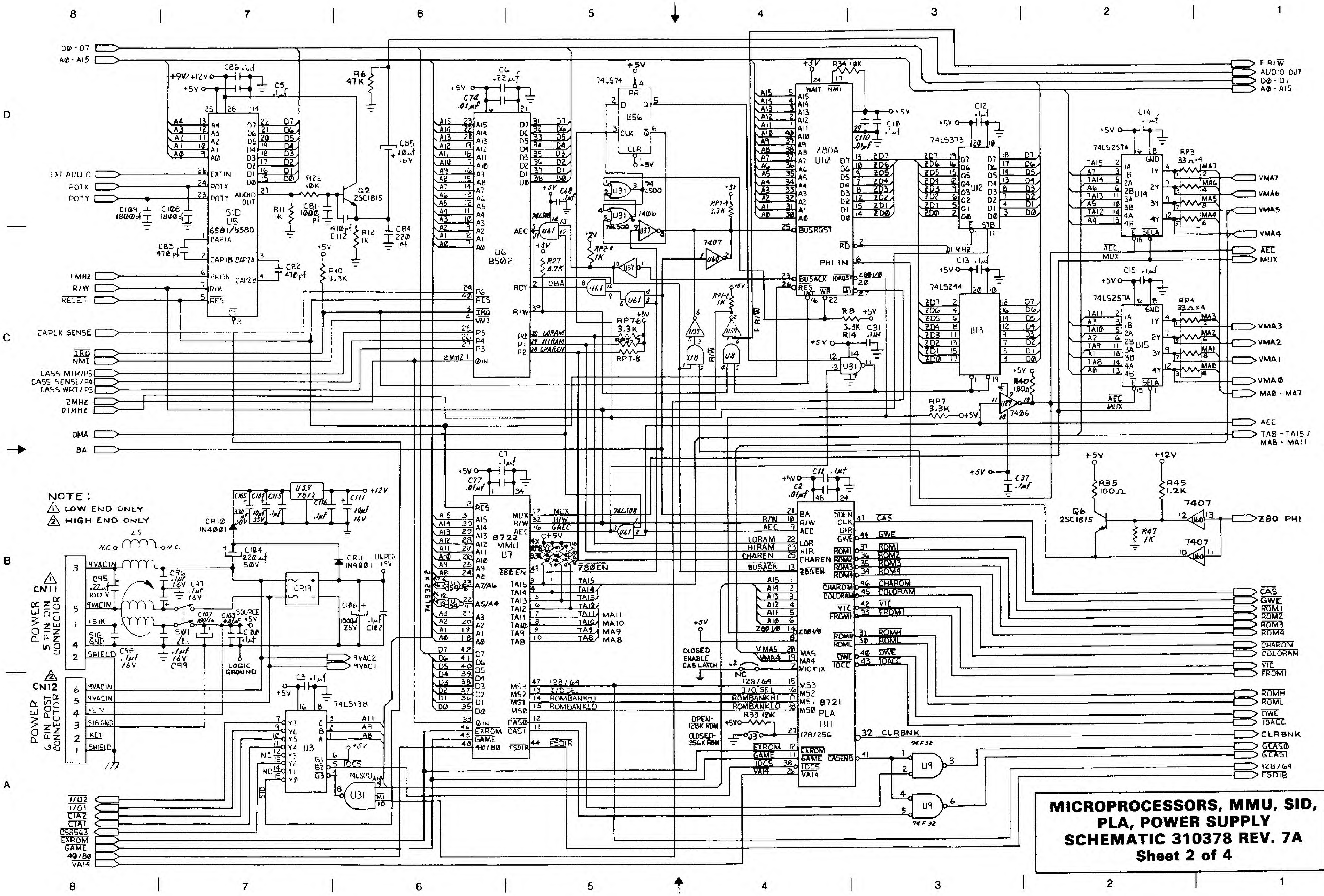
MISCELLANEOUS

Y1	16 MHz Clock Oscillator	325566-01
Y2	14.31818 Crystal	251467-01
L1-4	Inductor 2.2µH	
L5	Line Filter Assy	251878-01
FB1-15, 18-20	Ferrite Beads	
EMI1,2	EMI Filter	47pF
EMI3-6	EMI Filter	100pF
EMI9-11	EMI Filter	47pF
EMI12-35, 37,38	EMI Filter	100pF
EMI39	EMI Filter	270pF
EMI40-42	EMI Filter	100pF
EMI44-50	Ferrite Bead	
EMI69	EMI Filter	100pF
M1	Modulator	251917-01
SW1	Rocker Switch	252182-01
SW2	Push BT SPDT	251260-01
CN1	RT Angle Card Edge	906100-02
CN3,4	Mini D Cnnct Joy1,2	251057-01
CN5	Keybd Cnnct	252062-01
CN6	6 Pin Din Serial Cnnct Shld	252166-01
CN8	8 Pin Din Video Cnnct Shld	252168-01
CN10	D Cnnct 9 Pin Fem Rgbi	252024-01
CN11	5 Pin Square Din Shielded	252167-01
CN13	3 Pin Header .1 Center	
	Shield Box	326265-02
	Shield Cap	310407-01

QUICK REFERENCE

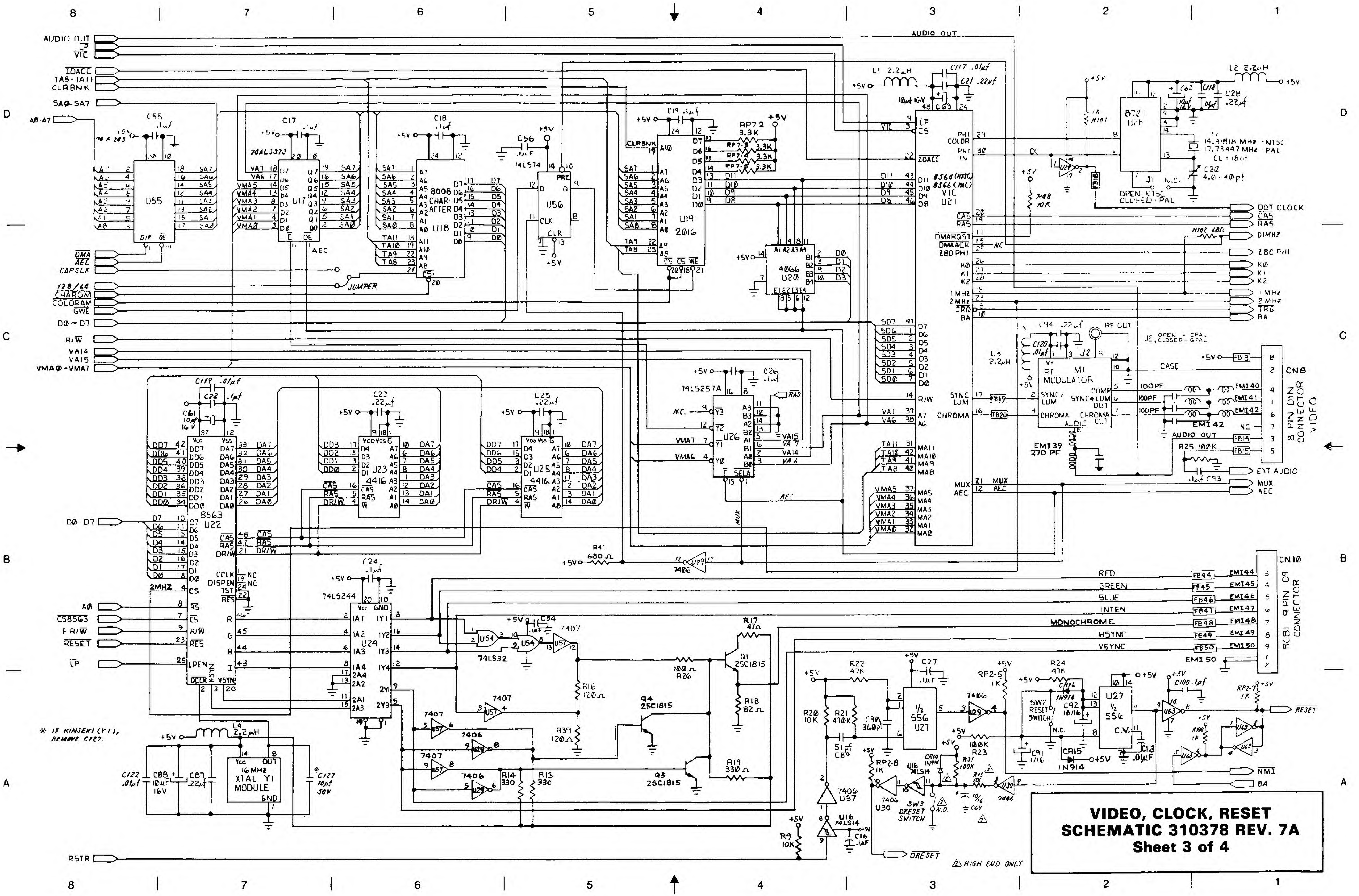
I/O — Control Ports, Keyboard, User Port, Serial Port, Cassette Port SCHEMATIC 310378 REV. 7 Sheet 1 of 4

QUICK REFERENCE



MICROPROCESSORS, MMU, SID, PLA, POWER SUPPLY SCHEMATIC 310378 REV. 7A Sheet 2 of 4

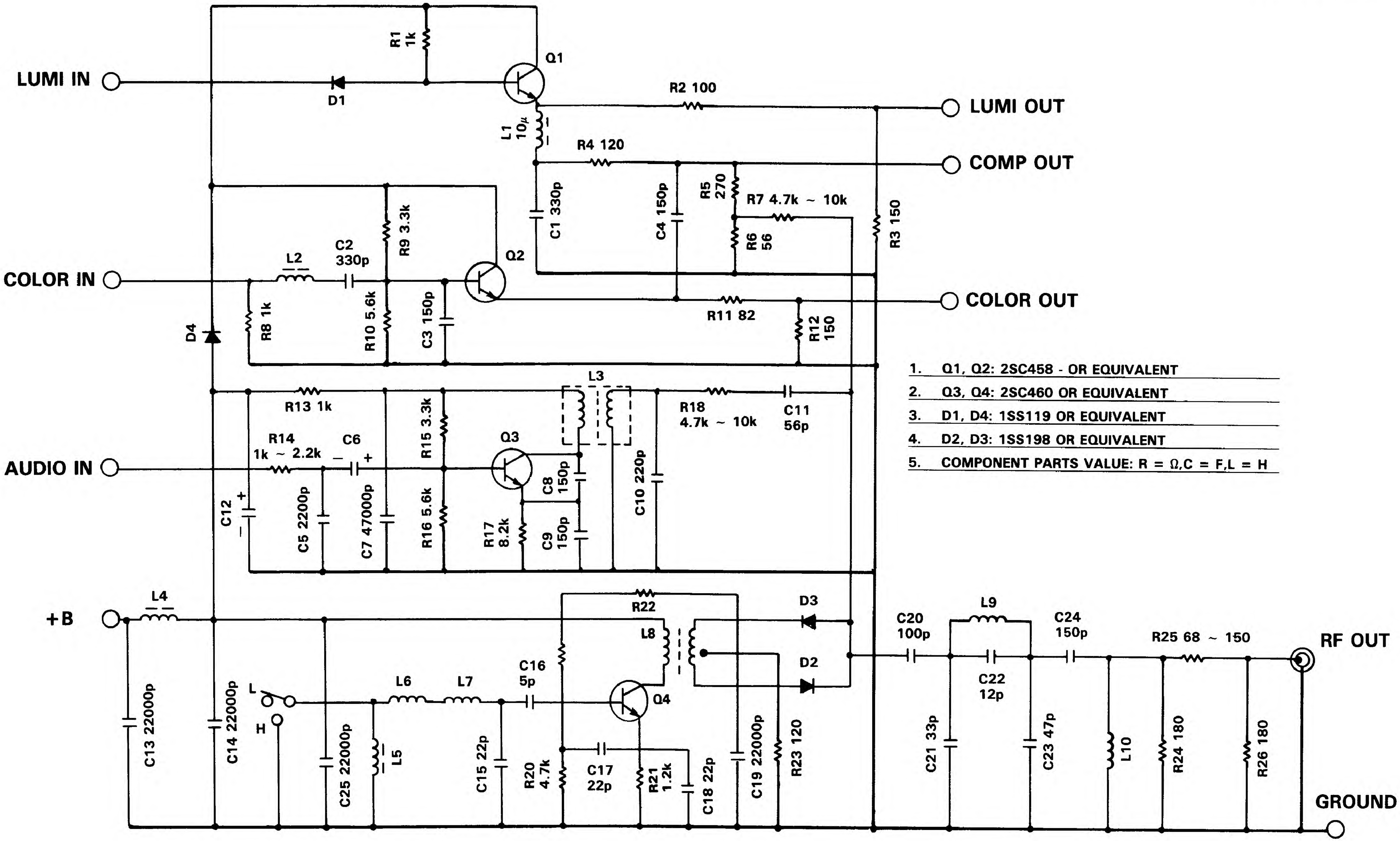
QUICK REFERENCE



VIDEO, CLOCK, RESET
SCHEMATIC 310378 REV. 7A
Sheet 3 of 4

QUICK REFERENCE

RAM, ROM
SCHEMATIC 310378 REV. 7
Sheet 4 of 4



1. Q1, Q2: 2SC458 - OR EQUIVALENT
2. Q3, Q4: 2SC460 OR EQUIVALENT
3. D1, D4: 1SS119 OR EQUIVALENT
4. D2, D3: 1SS198 OR EQUIVALENT
5. COMPONENT PARTS VALUE: R = Ω, C = F, L = H

FOR REFERENCE ONLY

POWER SUPPLY SCHEMATIC

MITSUMI — PN-252449-01

FOR REFERENCE ONLY

POWER SUPPLY SCHEMATIC

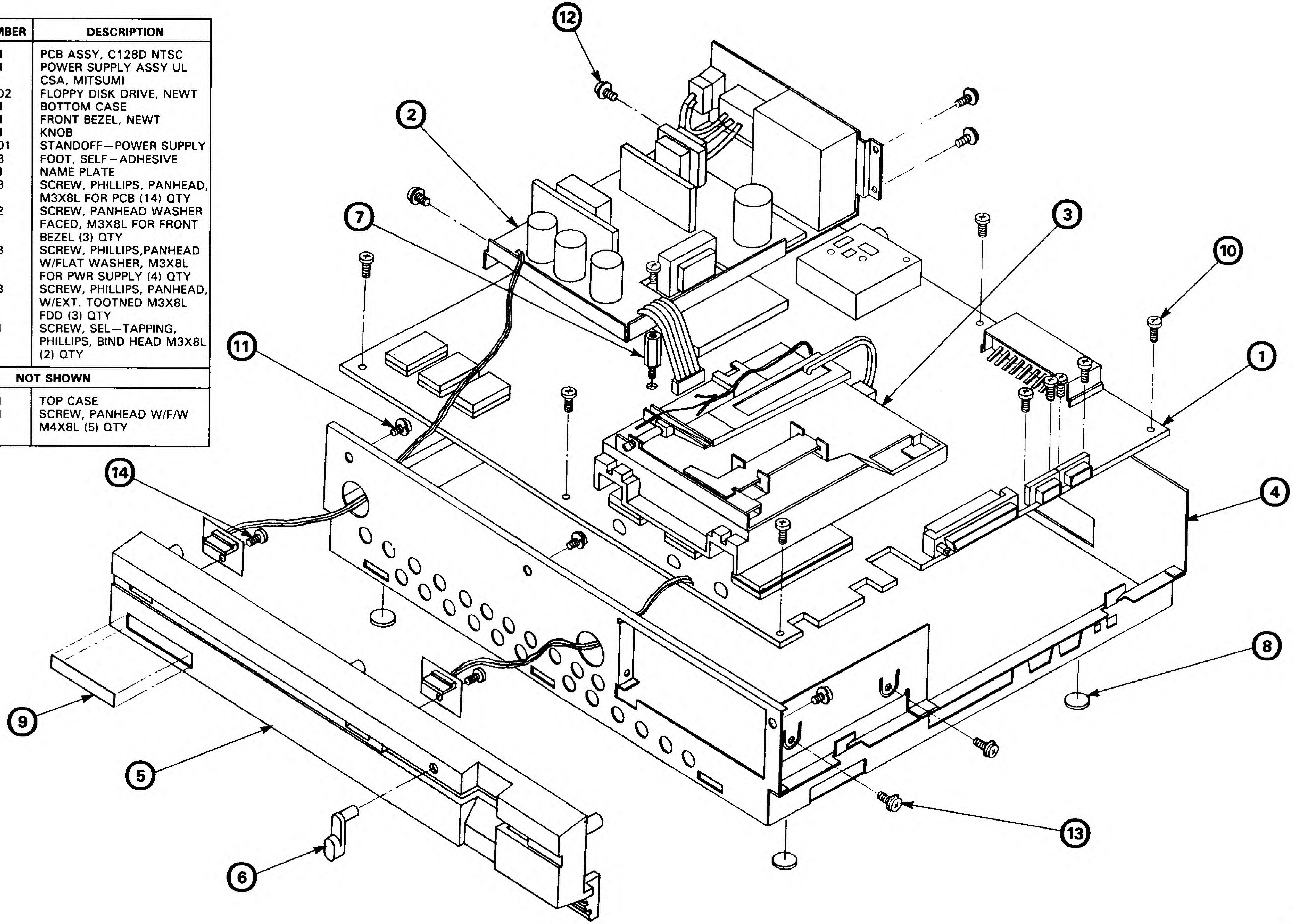
DEE-VAN — PN-252449-03

MAJOR PARTS LIST

PCB ASSY C128D NTSC	C250477-01
MANUAL — USERS	C354114-01
KEYBOARD ASSY NTSC	C250735-02
CASE TOP	C252454-01
CASE BOTTOM	C252455-01
BEZEL, FRONT NEWT	C252457-01
KNOB	C252050-01
DRIVE ASSY — NEWT	C252083-02
STAND-OFF	C252461-01
FOOT, SELF-ADHESIVE	C950150-01
NAMEPLATE	C251889-01
POWER SUPPLY ASSY UL, CSA MITSUMI	C252449-01
POWER SUPPLY ASSY UL, CAS DEE-VAN SUB FOR -01	252449-03
RF MODULATOR, PAL	252404-01
CARTRIDGE GUIDE	C326116-01
SHIELD BOX	C326265-01
SHIELD CAP ASSY	C310407-01
DISKETTE DEMO 1571	C252093-01
MANUAL — SERVICE	C314980-01

C - Indicates Commodore Stocked Part Number

ITEM	PART NUMBER	DESCRIPTION
1	250477-01	PCB ASSY, C128D NTSC
2	252449-01	POWER SUPPLY ASSY UL CSA, MITSUMI
3	2522083-02	FLOPPY DISK DRIVE, NEWT
4	252455-01	BOTTOM CASE
5	252457-01	FRONT BEZEL, NEWT
6	252050-01	KNOB
7	2522461-01	STANDOFF—POWER SUPPLY
8	950150-03	FOOT, SELF—ADHESIVE
9	251889-01	NAME PLATE
10	906800-03	SCREW, PHILLIPS, PANHEAD, M3X8L FOR PCB (14) QTY
11	906801-02	SCREW, PANHEAD WASHER FACED, M3X8L FOR FRONT BEZEL (3) QTY
12	325544-03	SCREW, PHILLIPS,PANHEAD W/FLAT WASHER, M3X8L FOR PWR SUPPLY (4) QTY
13	325541-03	SCREW, PHILLIPS, PANHEAD, W/EXT. TOOTNED M3X8L FDD (3) QTY
14	906883-01	SCREW, SEL—TAPPING, PHILLIPS, BIND HEAD M3X8L (2) QTY
		NOT SHOWN
	252454-01	TOP CASE
	350108-01	SCREW, PANHEAD W/F/W M4X8L (5) QTY

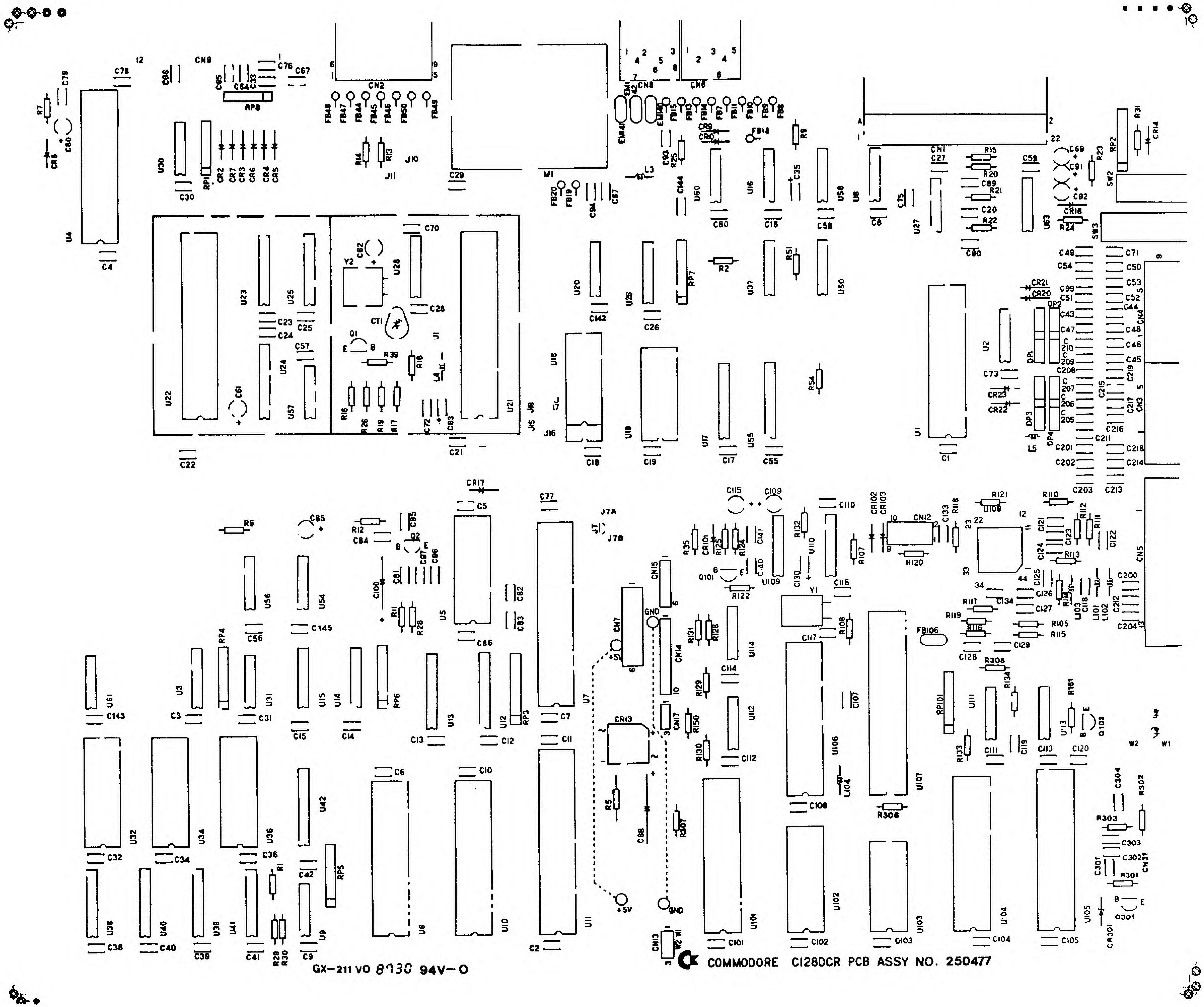


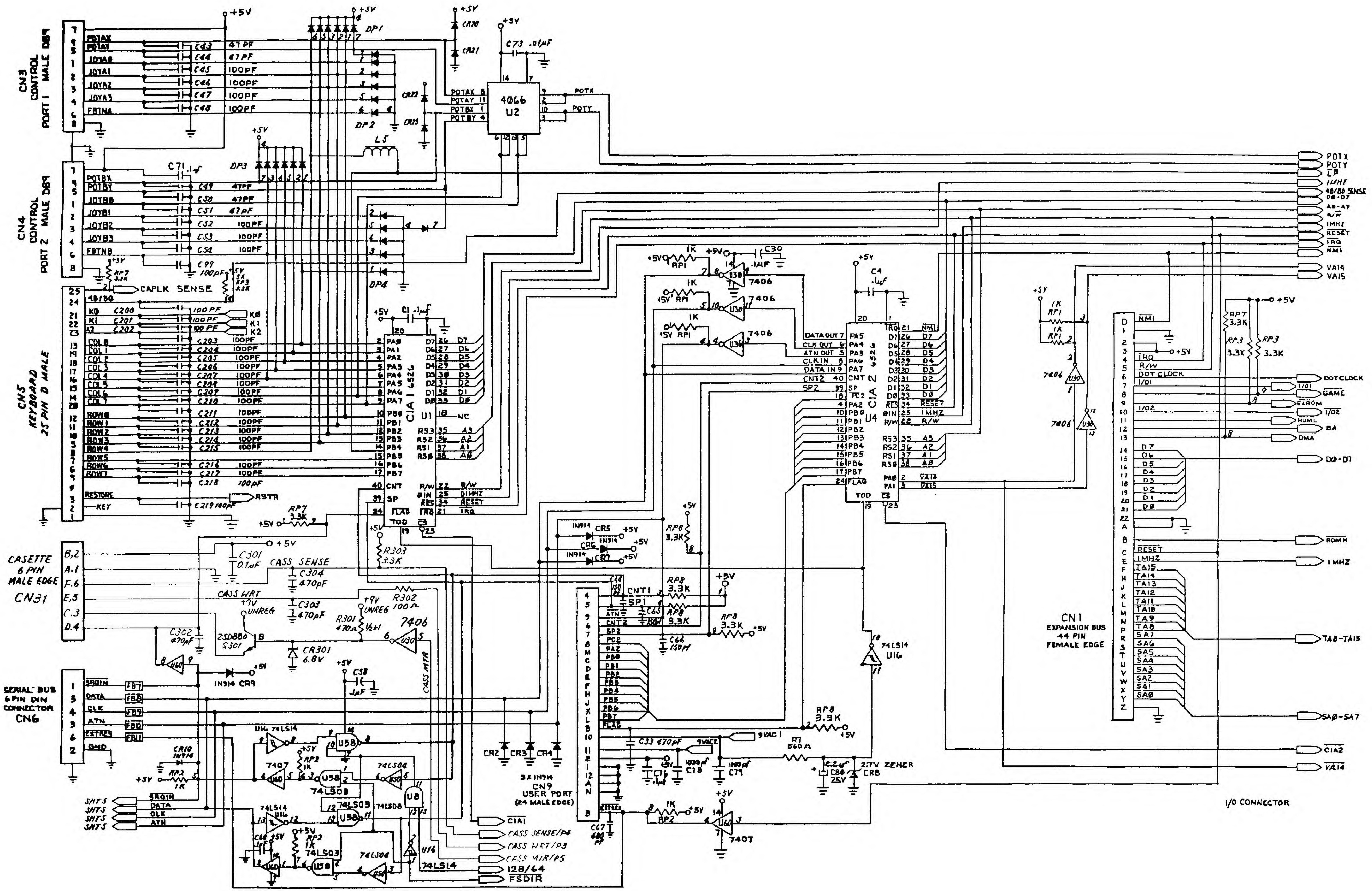
COMPONETS PARTS LIST

PCB ASSEMBLY #250477

U41	IC 64K X 4 DRAM	390083-02
U5	IC SID 8580	C318013-01
U21	IC VIC 8564 NTSC	C315009-01
U11	IC PAL 8721	C315012-01
U7	IC MMU 8722	C310389-01
U10	IC Z80 B 6MHZ	906150-02
U18	IC CHAR ROM	C315079-01
U27	IC NE556	901523-03
U19, 103	IC 2016 20LB 2K X 8	251637-05
U18	IC 8006 C128/C64 CHAR ROM	C390059-01
U2, 20	IC 4066	901502-01
U23, 25, 38-40	IC 64K X 4 DRAM 150NS	390083-02
U1, 4	IC 6526	C906108-01
U28	IC 8701	C251527-07
U6	IC 8502 MPU	C315020-01
U22	IC 8568 80 COL CRT CNTRL	C315092-01
U32	C128 ROM 2/3 (UK)	318023-02
U34	C128 ROM 1/4	C318022-02
U17	IC 74ALS373	390058-01
U55	74F245	252208-01
U9	74F32	390077-01
U107	FDC 5710	C252371-01
U104, 106	VIA 6522A 2MHZ	C901437-02
U104, 106 Sub.	IC 65SC22A 1MHZ	310653-01
U102	EP-ROM 27256 300NS	C252372-01
U108	FDD R/W AMP SONY CX20185	C252308-01
U108 Sub.	FDD R/W AMP MOTOROLA MC28719	252308-02
U108 Sub.	FDD R/W AMP SANYO LA8200	252308-03
U109	UPA2003C NEC	C251871-01
U109 Sub.	IC IR2C19 SHARP	251871-02
Q101	TRANS 2SA683	252400-01
Q301	TRANS 2SD880	902694-01
Q101 Sub.	TRANS MPSU51	310657-01
Q1, 2	TRANS 2SC1815	902693-01
DP1, 3	DIODE ARRAY 7 PIN	C252333-01
DP2, 4	DIODE ARRAY 7 PIN	C252333-02
CR301	DIODE ZENER RD 6.8 EB	900927-01
M1	RF MODULATOR NTSC	C252405-01
CT1	TRIMMER CAP 6.5 – 40P	C251029-02
SW1, 2	RESET BUTTON	C251260-01
CN5	CONNECTOR MALE 25 PIN	C359002-02

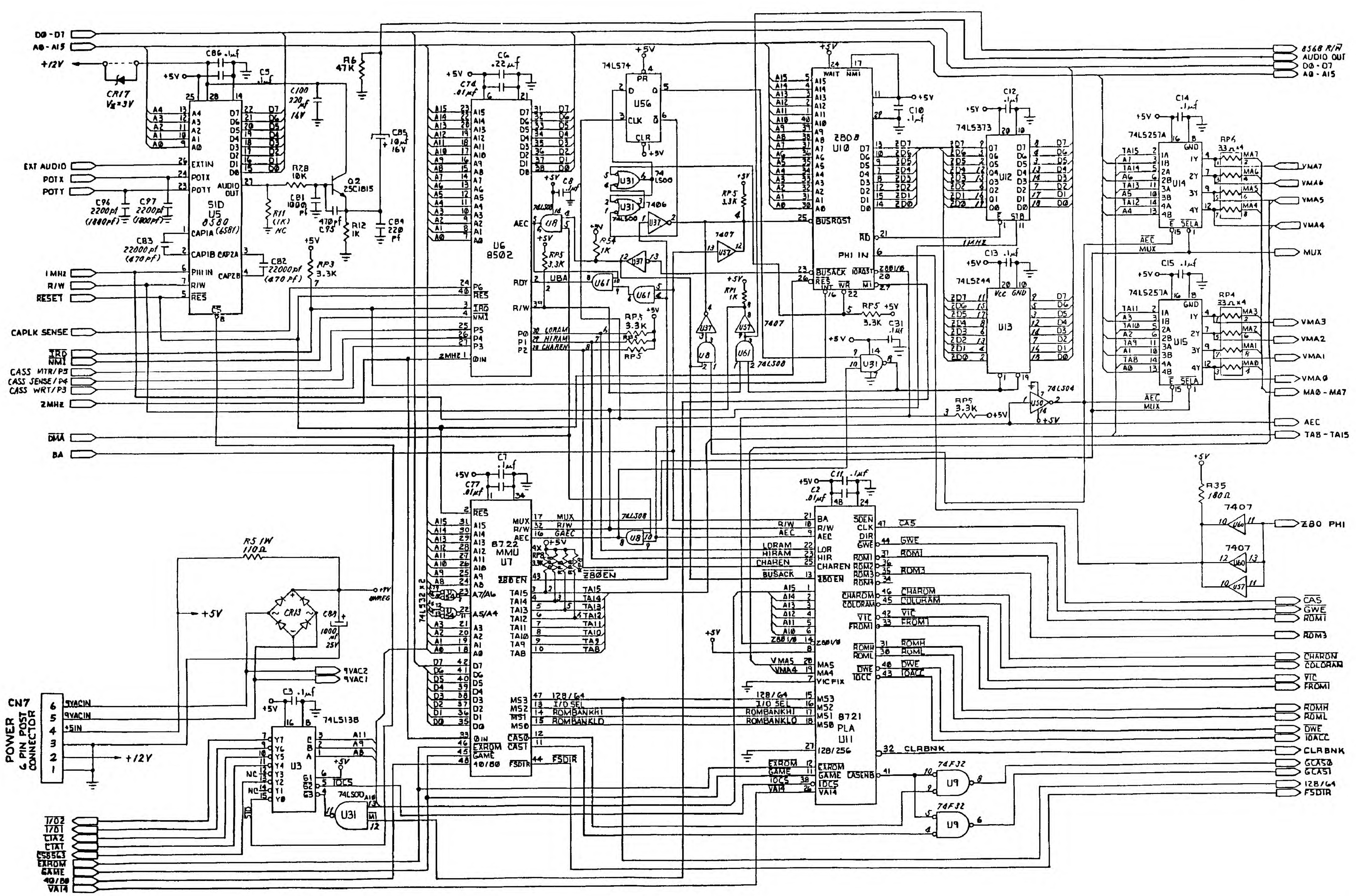
C-Indicates CBM Stocked Part Number


COMMODORE C128DCR PCB ASSY NO. 250477
GX-211 VO 8030 94V-O

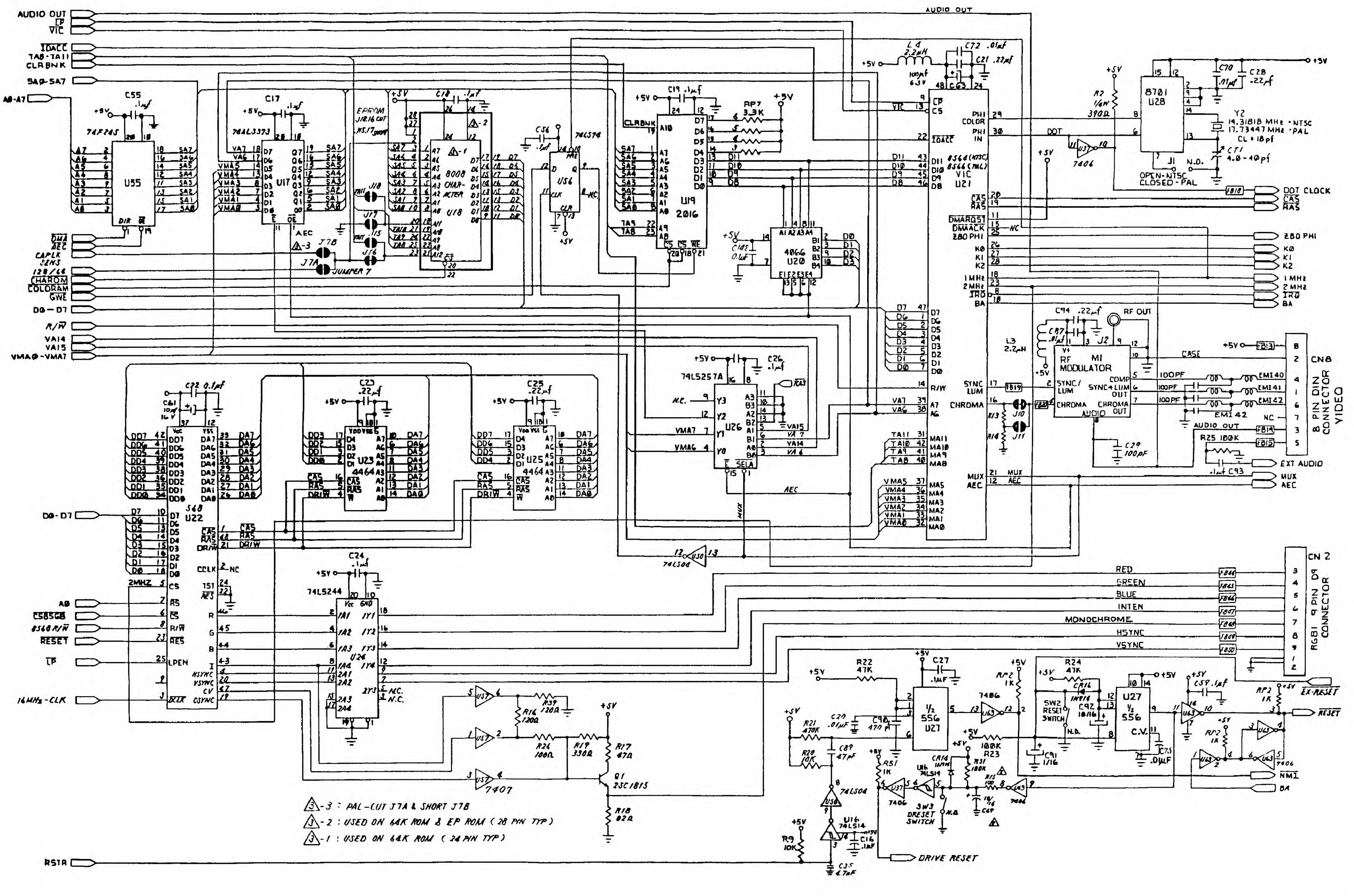

CN3 CONTROL PORT 1 MALE D89
CN4 CONTROL PORT 2 MALE D89
CN5 KEYBOARD 25 PIN D MALE
CASETTE 6 PIN MALE EDGE CN31
SERIAL BUS 6 PIN DIN CONNECTOR CN6
CIA 1 6526 U1
CIA 2 6526 U4
4066 U2
CN9 USER PORT (24 MALE EDGE)
CN1 EXPANSION BUS 44 PIN FEMALE EDGE
I/O CONNECTOR

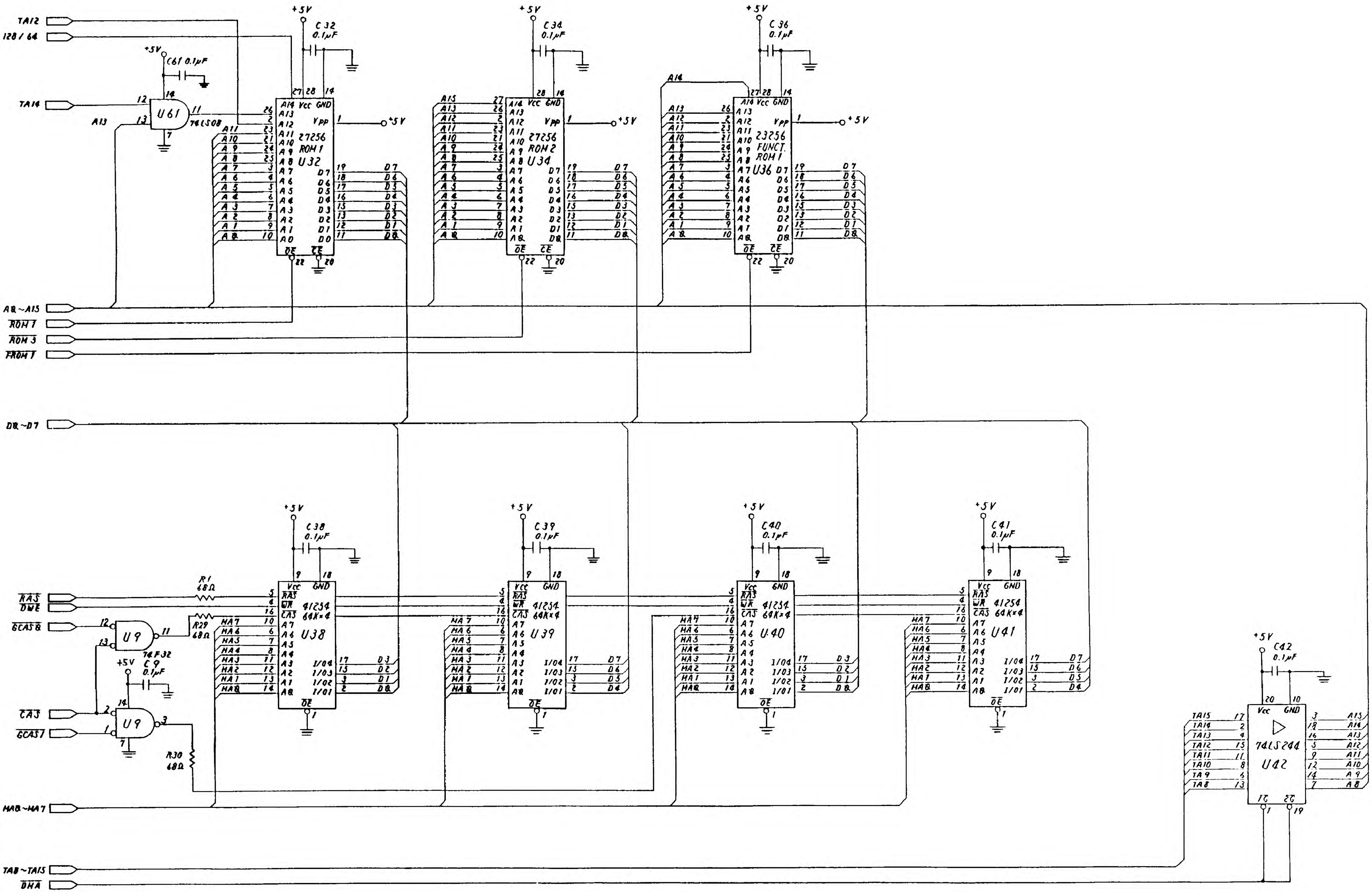
SCHEMATIC #252451

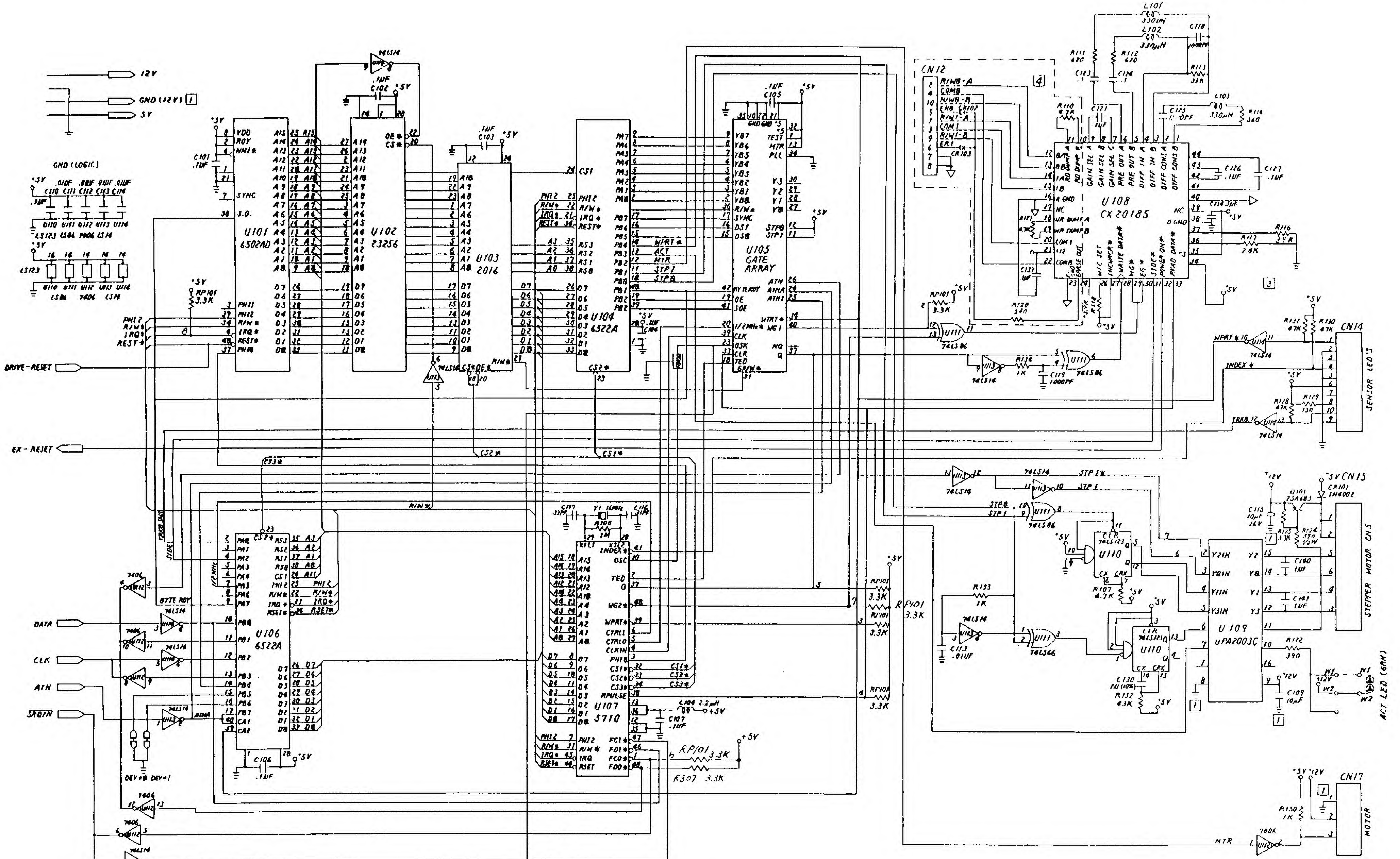
Sheet 2 of 5



SCHEMATIC #252451
Sheet 3 of 5







4 GND GUARD IS REQUIRED TO ELIMINATE NOISE FOR R/W HEAD.
3 XμF & XK VALUE WILL MEET FUJITSU R/W IC./ OPTION.
2 THIS SCHEMATIC MEETS NEWTRONICS D502 DISK DRIVE.
1 STEPPER GND: LOW IMPEADANCE GND CONNECTION IS REQUIRED BETWEEN EACH POINT TO ELIMINATE NOISE.
NOTES-UNLESS OTHERWISE SPECIFIED:

FDD CONTROL